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Wide tuning-range CMOS VCO based on a tunable active inductor

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In this paper, a wide tuning-range CMOS voltage-controlled oscillator (VCO) with high output power using an active inductor circuit is presented. In this VCO design, the coarse frequency is achieved by tuning the integrated active inductor. The circuit has been simulated using a 0.18-μm CMOS fabrication process and presents output frequency range from 100 MHz to 2.5 GHz, resulting in a tuning range of 96%. The phase noise is –85 dBc/Hz at a 1 MHz frequency offset. The output power is from –3 dBm at 2.55 GHz to +14 dBm at 167 MHz. The active inductor power dissipation is 6.5 mW and the total power consumption is 16.27 mW when operating on a 1.8 V supply voltage. By comparing this active inductor architecture VCO with general VCO topology, the result shows that this topology, which employs the proposed active inductor, produces a better performance.

Keywords: wide tuning range; voltage-controlled oscillator; active inductor; phase noise; output power

1. Introduction

The expansion of wireless communication systems (such as 3G cellular phones, wireless LAN, WPAN, RFID tags, GSM and CDMA) demands for low cost, high performance, small size and low power-integrated Radio Frequency (RF) transceivers. One of the challenging tasks in the design of RF transceiver is to implement a fully integrated voltage-controlled oscillator (VCO) with a wide tunable frequency range.

In RF transceiver designs, VCO is an important building block for frequency translation. The necessary performance criterion of the VCO for use in RF wireless application is low phase noise and a wide tuning range. In a conventional VCO topology, a passive spiral inductor is used to tune the VCO LC-tank. However, integrated passive spiral inductors have many disadvantages such as large area and a low quality factor (Q). These issues can be addressed by using a high quality factor active inductor (AI). The result is a decrease in circuit area and an increase in the inductance quality factor. Another advantage of the AI is an expansion in the tuning range. In a conventional VCO topology, the tuning range is achieved by changing the varactor capacitors within the LC-tank circuit. The changing ratio of the varactor is determined by the maximum-to-minimum capacitance ratio of the varactor ($C_{\mathrm{var,max}}/C_{\mathrm{var,min}}$). For typical varactor capacitance ratios, the tuning range of an LC-tank VCO is limited to 30% (Lu, Hsieh, & Liao, 2006). To overcome the limitation of a restricted tuning range, an AI-based VCO is introduced. In this paper, a

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novel circuit topology is proposed for a tunable AI. In the proposed circuit topology, the inductance can be adjusted to different values over a wide frequency range. The total frequency tuning range is 96%. Therefore, this VCO is very suitable for standard RF transceiver design.

This paper is organised as follows. Section 2 describes the design of AI circuit topology, and Section 3 presents a wide tuning range VCO. Section 4 provides circuit simulation results and finally, conclusions are given in Section 5.

2. Active inductor architecture

CMOS AIs are commonly realised by using a gyrator-C topology as shown in Figure 1 (Bucossi & Becker, 2008; Fillaud & Barthelemy, 2008; Ismail & Olsson, 2003; Vema Krishnamurthy, El-Sankary, & El-Masry, 2010; Wei, Chiu, & Feng, 2005; Yang, Hsieh, & Tsai, 2010). It is composed of two transconductors G_{m1} and G_{m2} connected in feedback configuration, whilst C_1, g_1, C_L and g_L are the parasitic capacitances (C) and conductances (g) at nodes 1 and 2, respectively. The input admittance of the gyrator circuit Y_{in} is (Yuan, 2008):

$$Y_{\text{in}} = \frac{1}{Z_{\text{in}}} = g_1 + sC_1 + \frac{G_{m1}G_{m2}}{sC_L + g_L} \tag{1}$$

The gyrator circuit can be modelled by a resonator as shown in Figure 1. R, L and C are given by

$$L = \frac{C_L}{G_{m1}G_{m2}},\ R = \frac{g_L}{G_{m1}G_{m2}},\quad C = C_1,\quad g_p = g_1 \tag{2}$$

The proposed AI circuit is shown in Figure 2(a), whilst Figure 2(b) shows the small-signal equivalent circuit of the AI.

The input admittance, Y_{in}, which is derived from an analysis of the small-signal AC equivalent, is

$$Y_{\text{in}} = C_1 \cdot s + g_{ds4} + Y_{\text{in2}} \tag{3}$$

$$Y_{\text{in2}} = \frac{C_2C_3C_4s^3 + \alpha s^2 + \beta s + \gamma}{C_2C_3C_4R_f s^3 + \delta s^2 + \varepsilon s + \theta} \tag{4}$$

where α, β, γ, δ, ε and θ are

$$\alpha = C_2C_4g_{m3} + C_2C_3g_{m4} + C_3C_4g_{ds1} + C_3C_4g_{m1} \tag{5}$$

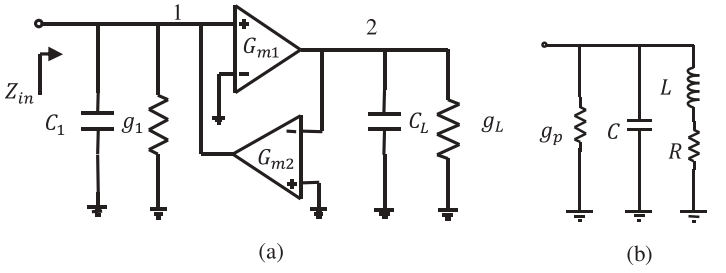


Figure 1. (a) Gyrator circuit block diagram. (b) Equivalent RLC model of gyrator.

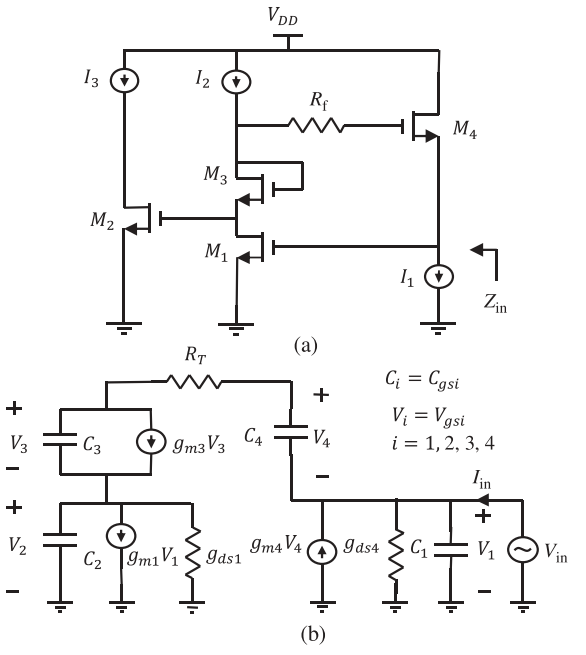


Figure 2. (a) AI circuit. (b) Small-signal equivalent circuit.

$$\beta = C_2 g_{m3} g_{m4} + C_4 g_{m3} g_{ds1} + C_4 g_{m1} g_{m3} + C_3 g_{m4} g_{ds1} + C_3 g_{m1} g_{m4} \tag{6}$$

$$\gamma = g_{m3} g_{m4} g_{ds1} + g_{m1} g_{m3} g_{m4} \tag{7}$$

$$\delta = C_2 C_4 g_{m3} R_f + C_2 C_3 + C_3 C_4 g_{ds1} R_f + C_2 C_4 + C_3 C_4 \tag{8}$$

$$\varepsilon = C_2 g_{m3} + C_4 g_{m3} g_{ds1} R_f + C_3 g_{ds1} + C_4 g_{ds1} + C_4 g_{m3} \tag{9}$$

$$\theta = g_{m3} g_{ds1} \tag{10}$$

where $C_i = C_{gsi}$ (i = 1, 2, 3, 4).

According to (3), R_s and L_{eq} can be extracted from real and imaginary part of Z_{in2} at low frequency, respectively.

When $Z_{in2} = \frac{1}{Y_{in2}}$ and we assume that $g_{ds1} \ll g_{m1}$, then

$$R_s = \mathrm{Re}[Z_{in2}(j\omega)] \approx \frac{g_{m3} g_{ds1}}{g_{m3} g_{m4} g_{ds1} + g_{m1} g_{m3} g_{m4}} \approx \frac{g_{ds1}}{g_{m1} g_{m4}} \tag{11}$$

$$L_{eq} = \mathrm{Im}[Z_{in2}(j\omega)] \approx \frac{C_2 g_{m3} + C_4 g_{m3}(1 + g_{ds1} R_f) + g_{ds1}(C_3 + C_4)}{g_{m3} g_{m4} g_{ds1} + g_{m1} g_{m3} g_{m4}} \approx \frac{C_2 + C_4(1 + g_{ds1} R_f)}{g_{m1} g_{m4}} \tag{12}$$

Equation (12) shows that the value of inductance can be controlled by varying R_f. Typically ($1 + g_{ds1} R_f$) is designed to be a value greater than unity. In this design, g_{ds1} = 0.45 mA/V, g_{m1} = 5.2 mA/V and R_f is variable from 0.5kΩ to 20kΩ; in this case

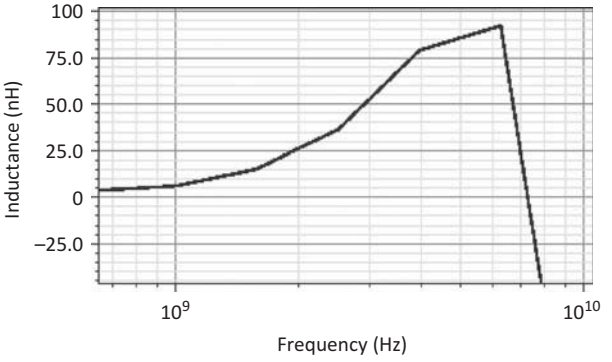


Figure 3. The simulated inductance of AI.

$(1 + g_{ds1}\ R_f)$ will be variable from 1.225 to 9. This means that the inductance will be increased by increasing the factor of $(1 + g_{ds1}\ R_f)$.

And also according to (3), C_{eq} is equal to $C_1 = C_{gs1}$ and R_p is $\frac{1}{g_{ds4}}$.

The quality factor, Q, is (Yuan, 2008)

$$Q = \left(\frac{\omega L_{eq}}{R_s}\right) \frac{R_p}{R_p + R_s\left[1 + \left(\frac{\omega L_{eq}}{R_s}\right)^2\right]} \left[1 - \frac{R_s^2 C_p}{L_{eq}} - \omega^2 L_{eq} C_p\right] \tag{13}$$

According to Equations (11), (12) and (13), R_f, g_{m1}, g_{m3}, g_{m4} and g_{ds1} have very important effect on quality factor.

The AI circuit has been simulated with Cadence Virtuoso Spectre using a 0.18-µm Silterra CMOS technology. The inductance plot is shown in Figure 3. From this simulation, the best operating frequency for this L is 1–7 GHz. According to Figure 3, the peak value of L happened around 5.5 GHz. But by changing bias condition, this peak value will be changed. And also, by adjusting L, the frequency of peak point will be changed. The best performance of this circuit topology is linearity and adjustability range for L. Inductance can vary from a few nH to 100 nH. It can be adjusted to fixed value to suit frequency variations for a specific range. Feedback resistance, R_f connected to M_4 acts as an additional inductance looking into the source terminal of M_4 (Mukhopadhyay et al., 2005; Wei et al., 2005; Yang et al., 2010; Yuan, 2008).

3. VCO design using AIs

Figure 4 shows the proposed VCO circuit. It is composed of two AIs in a cross-coupled configuration. In Figure 4, M_1, M_2, M_3, M_4, M_{10}, M_{11}, M_{12} and M_{13} are the main transistors within the AI, and M_5, M_6, M_7, M_8, M_9, M_{14}, M_{15}, M_{16}, M_{17} and M_{18} are the current source transistors for biasing AIs circuit. M_{19} and M_{20} are the cross-coupled configuration transistors.

The total parasitic capacitance of VCO is

$$C_{total} = C_{gsNR} + C_{eq} \tag{14}$$

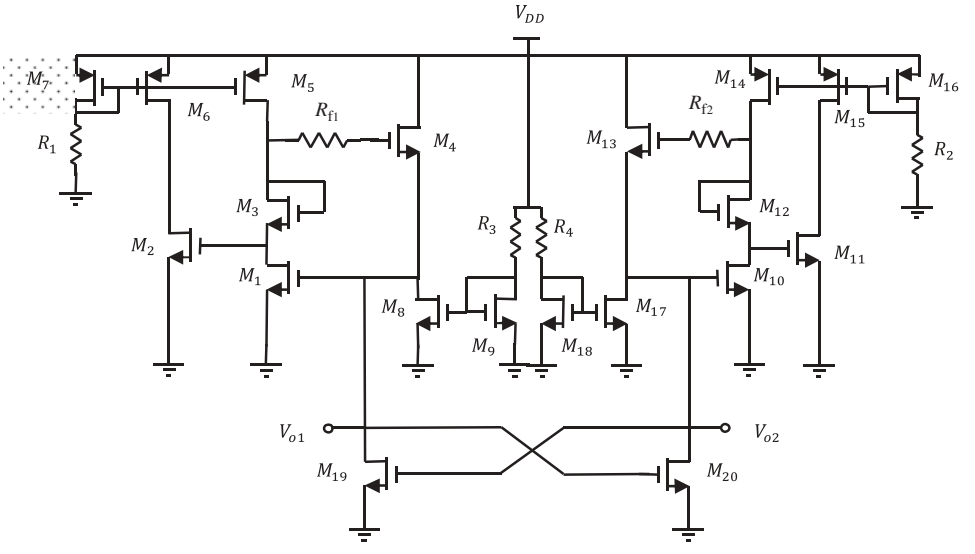


Figure 4. Schematic of proposed LC-tank VCO based on AIs.

where C_{gsNR} is the gate-source capacitance of the cross-coupled negative resistance.

The oscillation frequency is

$$\omega_0 = \frac{1}{\sqrt{L_{\text{eq}}.C_{\text{total}}}} \tag{15}$$

According to (Hajimiri & Lee, 1998, 2003) the total single-sideband phase noise spectral density of the VCO, £(Δω), is given by

$$\pounds(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\sum_{n=0}^{\infty} C_n^2}{4q_{\max}^2\Delta\omega^2}\right) \tag{16}$$

According to Parseval's equation:

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi} \left|\Gamma(x)\right|^2 \mathrm{d}x = 2\Gamma_{\text{rms}}^2 \tag{17}$$

where Γ_{rms} is the rms value of $\Gamma(x)$. Then, we have

$$\pounds(\Delta\omega) = 10\log\left(\frac{\Gamma_{\text{rms}}^2}{q_{\max}^2}.\frac{\frac{\overline{i_n^2}}{\Delta f}}{2\Delta\omega^2}\right) \tag{18}$$

This equation is the phase noise spectrum of an arbitrary oscillator in $1/f^2$ region of the phase noise spectrum. In this equation, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) of the oscillator, $q_{\max}$ is the maximum charge displacement across the capacitor on the node, Δω is the offset frequency and $\frac{\overline{i_n^2}}{\Delta f}$ is the total output noise.

According to Equation (19), the total output noise, $\frac{\overline{\iota_n^2}}{\Delta f}$, is the sum of current noise of AI part and the negative resistor.

$$\frac{\overline{\iota_{n,\text{total}}^2}}{\Delta f} = \frac{\overline{\iota_{n,\text{AI}}^2}}{\Delta f} + \frac{\overline{\iota_{n,\text{NR}}^2}}{\Delta f} \tag{19}$$

$\frac{\overline{\iota_{n,\text{AI}}^2}}{\Delta f}$ is current noise part of AI and $\frac{\overline{\iota_{n,\text{NR}}^2}}{\Delta f}$ is current noise of negative resistance. The noise current of a MOSFET is modelled by channel-induced noise and gate-induced noise as:

$$\left(\frac{\overline{\iota_n^2}}{\Delta f}\right) = 4KT\gamma g_{ds} + 4KT\delta g_m \tag{20}$$

where g_{ds} and g_m are the output conductance and transconductance, K is Boltzmann's constant, $\gamma \approx 2$ and $\delta \approx 4$ for short channel devices. To reduce the phase noise of AI part, g_{m1} and g_{m4} should be reduced. In this case, according to (12), L_{eq} will be increased which lead to reduction in oscillation frequency. There is a trade-off between phase noise and oscillation frequency.

4. Simulation results

The proposed circuit is simulated with Cadence Spectra in 0.18-μm CMOS technology. The designed VCO circuit requires 9.041 mA current from 1.8 V power supply voltage. In this circuit, R_{f} is a very effective element to control the centre frequency. By sweeping R_{f} from 0.2 kΩ to 1 MΩ, the output frequency changes from 2.55 GHz to 78 MHz. Figure 5 shows the variation of output frequency versus R_{f}. Figure 6 plots the output power of the VCO for $R_{\text{f}} = 5$ kΩ. The oscillation frequency for $R_{\text{f}} = 5$ kΩ is 1.4 GHz. In addition, the variation of output power and phase noise according to the R_{f} variation are shown in Figure 7.

As shown in Figure 7(a), the maximum and minimum output power is +14 dBm at 80 MHz (for $R_{\text{f}} = 750$ kΩ) and –0.3 dBm at 2.55 GHz (for $R_{\text{f}} = 0.3$ kΩ), respectively. This shows that by increasing R_{f}, the VCO output frequency decreases dramatically but output power increases slowly. Also, by increasing R_{f}, the phase noise decreases slowly. This means that there is a trade-off between the feedback resistance, phase noise and output power. According to Figure 7(b), the maximum and minimum phase noise are –80 dBc/Hz at 2.37GHz and –93 at 828 MHz, respectively.

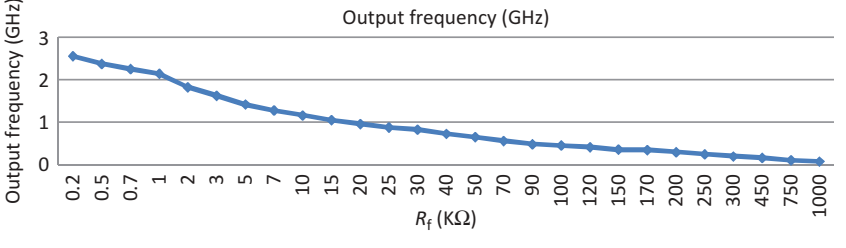


Figure 5. VCO output frequency tuning with R_{f}.

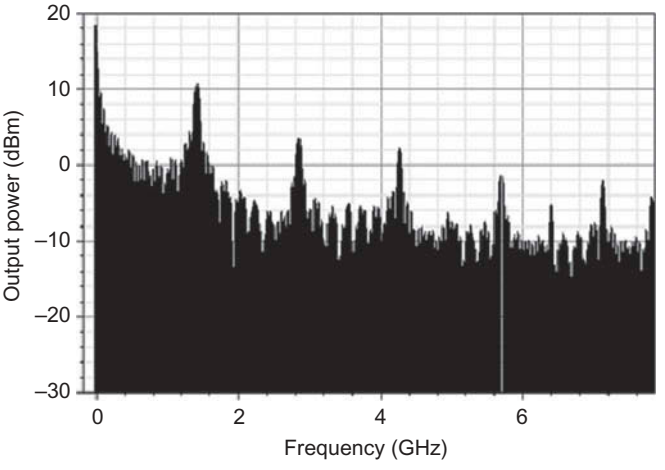


Figure 6. VCO output power for R_f = 5 kΩ.

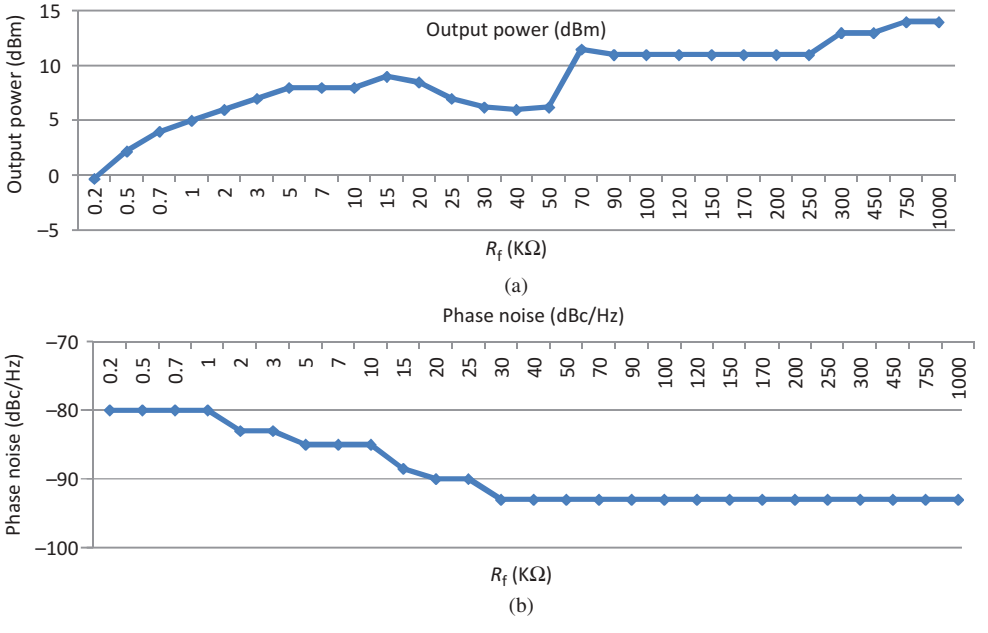
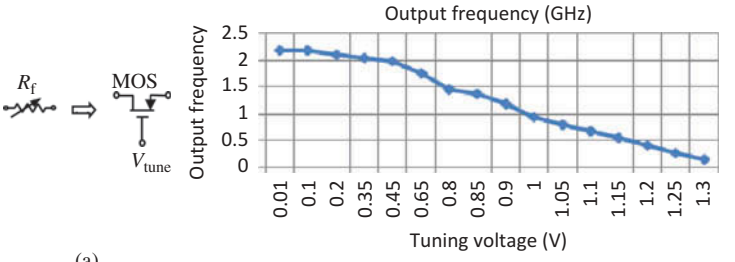


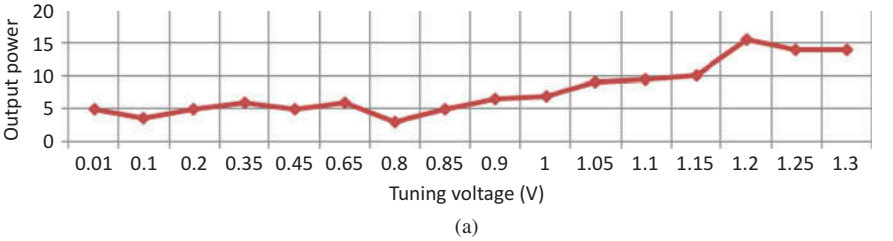
Figure 7. (a) VCO output power variations according to R_f variations. (b) Phase noise variations according to R_f variations at 1 MHz offset frequency.

The variable resistor can be implemented by a PMOS transistor, as shown in Figure 8(a). The gate-source voltage control changes the resistance value. The tuning voltage varies from 0.1 V to 1.3 V and output frequency, which is extracted from the post-simulation of the VCO layout including GSG (Ground-Signal-Ground) pad and parasitic capacitors, varies from 2.3 GHz to 0.1 GHz as shown in Figure 8(b). Figure 9(a) and (b) shows the output power and the phase noise of VCO by variation of tuning voltage (V_t), respectively.

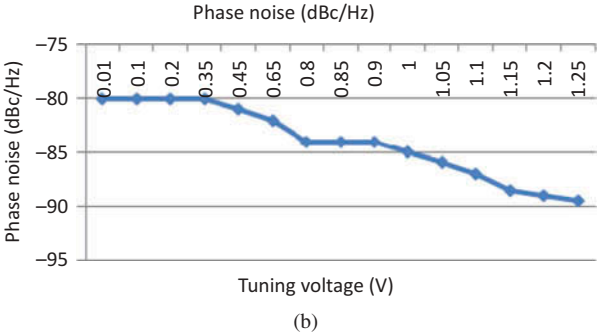


(a) (b)

Figure 8. (a) Tunable PMOS resistance. (b) Variation of VCO output frequency by tuning V_t.



(a)



(b)

Figure 9. (a) Variation of VCO output power for different tuning voltage (V_t). (b) Variation of phase noise for different tuning voltage (V_t) at 1 MHz offset frequency.

Figure 10 shows the layout of the VCO circuit. The total size is 80 µm × 120 µm (without GSG pad). The summarised characteristics of the VCO from the simulation results are shown in Table 1. Table 2 compares this circuit with recently published VCOs. The characteristics of this VCO highlight its higher tuning-range and output power spectrum.

5. Conclusion

A wide tuning-range AI-based VCO has been developed and implemented in 0.18-µm CMOS technology. The tuning-range frequency is from 0.1 GHz to 2.5 GHz and output power is from +5 dBm to +15 dBm, whilst phase noise variation is from –80 dBc/Hz to –93 dBc/Hz at 1 MHz frequency offset. The total power dissipation is 16.27 mW.

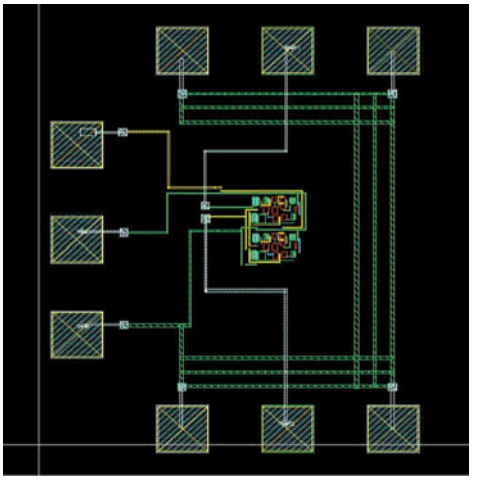


Figure 10. VCO circuit layout with GSG pad.

Table 1. Performance summary of wide tuning-range VCO.

Technology	0.18-µm CMOS
Tuning range	0.1–2.5 GHz
K_{VCO}	2600 MHz/V
V_{DD}	1.8 V
DC power (total)	16.27 mW
DC power (AI core)	6.5 mW
Output power level	+5 dBm to +15 dBm
Phase noise at 1 MHz	–80 dBc/Hz to –93 dBc/Hz
Active area	80 µm × 120 µm
Tuning-range technique	Active inductor

Table 2. Comparison of published CMOS VCOs.

Ref.	Process CMOS	Tuning range (GHz)	K_{VCO} (MHz/V)	Power diss. (mW)	Output power (dBm)	Chip area µm^2
Tzey et al. (2010)	0.18-µm CMOS	1.26–2.98	–	44.6	–5.3 to –18.7	585 × 679
Wei et al. (2005)	0.18-µm CMOS	2.7–5.4	–	18.4	–13.8 to –20.6	600 × 675
Lu et al. (2006)	0.18-µm CMOS	0.5–3	2500	6–28	–14 to –22	150 × 300
Mukhopadhyay et al. (2005)	0.18-µm CMOS	0.5–2	500	13.8	–21 to –29	300 × 300
This work	**0.18-µm CMOS**	**0.1–2.5**	**2600**	**16.27**	**+5 to +15**	**80 × 120**

References

Bucossi, W., & Becker, J. P. (2008). Practical considerations in the Use of CMOS active inductors. *IEEE Topical Meeting on Silicon In RF Systems*, 90–93.

Fillaud, M., & Barthelemy, H. (2008). Design of a wide tuning range VCO using an active inductor. *2008 Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference*, *2*, 13–16.

Hajimiri, A., & Lee, T. H. (1998). A general theory of phase noise in electrical oscillators. *IEEE Journal of Solid-State Circuit*, *33*(2), 179–194.

Hajimiri, A., & Lee, T. H. (2003). *The design of low noise oscillator*. Norwell, MA: Kluwer.

Ismail, M., & Olsson, H. (2003). RF bandpass filter design based on CMOS active inductors. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 50*(12), 942–949.

Lu, L. H., Hsieh, H. H., & Liao, Y. T. (2006). A wide tuning-range CMOS VCO with a differential tunable active inductor. *IEEE Transactions on Microwave Theory and Techniques, 54*(9), 3462–3468.

Mukhopadhyay, R., Park, Y., Sen, P., Srirattana, N., Lee, J., Lee, C. H., … Laskar, J. (2005). Reconfigurable RFICs in Si-based technologies for a compact intelligent RF front-end. *IEEE Transactions on Microwave Theory and Techniques, 53*(1), 81–93.

Vema Krishnamurthy, S., El-Sankary, K., & El-Masry, E. (2010). Noise-cancelling CMOS active inductor and its application in RF band-pass filter design. *International Journal of Microwave Science and Technology,* 1–8.

Wei, C. C., Chiu, H. C., & Feng, W. S. (2005). An ultra-wideband CMOS VCO with 3–5 GHz tuning range. *IEEE International Workshop on Radio-Frequency Integration Technology*, November 30–December *2*, Singapore.

Yang, J. -T., Hsieh, S. -K., & Tsai, P. -J. (2010). A wide tuning range voltage-controlled oscillator with active inductors for bluetooth applications. *Proceedings of the 4th International Conference on Circuits, Systems and Signals, Stevens Point, WI: World Scientific and Engineering Academy and Society (WSEAS)*.

Yuan, F. (2008). *CMOS active inductors and transformers principle, implementation, and applications*. Berlin: Springer.