2020 8th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions) (ICRITO)
Amity University, Noida, India. June 4-5, 2020

Ultra Low power SRAM Cell for High Speed Applications using 90nm CMOS Technology

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***Abstract*- SRAM is employed as a cache memory within the processor associate degree additionally has an application of the integrated system. With the continuing advancement of microcircuit technology, the density of SRAMs in embedded applications has adult well in recent years. The power dissipation of the projected new SRAM cell is sort of stable for top speed operations. Since the amount of transistors and therefore the space has exaggerated compared to the standard SRAM 6T cell, this disadvantage will simply be overcome by low power dissipation even at terribly high frequencies. During this paper, we have a tendency to propose a replacement low-power SRAM model for high speed operations. This new style approaches the voltage mode methodology to scale back voltage swing around writing switch activity. Within the standard SRAM cell thanks to method variation, the hold on knowledge is also destroyed throughout the read operation. As a result, the outpouring current thanks to bigger power dissipation is reduced. Dynamic power is calculated for various frequencies and compared to the standard SRAM 6T cell. During this proposed methodology, the new SRAM cell may be accustomed offer low-power consumption of high-speed devices like laptops, smart phones, programmable logic devices, and so on. The results of the simulations show that the frequency of the projected SRAM model additionally will increase; the facility dissipation is almost constant. This ensures reduced energy dissipation for prime frequency SRAM CMOS cell layout. The projected style is simulated on the LT SPICE IV using 90nm CMOS technology.**

Keywords: CMOS, SRAM, Low Power, VTC, Dynamic Power, BL, WL.

I. INTRODUCTION

SRAM contends a key role in low-power VLSI devices for high-quality applications. Among several integrated memory technologies, SRAM is in an exceedingly position to produce most performance whereas maintaining low power consumption of standby [1]. Reducing power consumption makes the tool load reliable. One among the most drivers of CMOS technology was the necessity for devices that consume little or no power. As a result, CMOS devices are higher of their low power consumption. However, to reduce the necessity for a system for a tool, it's difficult to know that CMOS devices consume less power than comparable totally different technology devices [2]. The method of low consumption has become a necessary a part of VLSI style, particularly for high-speed systems [3]. In general, the dynamic characteristics management the energy dissipation in most digital systems. The dynamic dissipation of capacitance in the main depends on the frequency of modification, the voltage and therefore the voltage fluctuation ensuing. Reducing the availability voltage is that the easiest method to scale back dynamic energy dissipation. Sadly, low current voltage greatly reduces performance [4]. Low voltage reduces the utmost voltage, that will increase this minimum current or discharge current that will increase the dissipation of static energy. The limitation of fluctuations within the output voltage corresponds to a decrease in dynamic power and delays. The SRAM-based cache is best for applications running on the system as a result of its high speed and low power consumption. Therefore, SRAM is employed for mobile tools [5]. SRAM could be a volatile memory designed as static RAM for high-speed low-power devices with blessings in each active and sleep mode [6]

II. RELATED WORK

Bhattacharya et al planned mixed-mode detector electronic equipment that has been changed for low-power SRAM applications with CMOS one hundred eighty nm technology. To beat the constraints of the standard mixed mode sensory electronic equipment in terms of detection delay, the information line division was created additional quickly by preventing part discharging the BL line within the planned topology [7]. SRAM analysis is considered for static power down, storage voltage, read limit (RM) and write limit (WM) for low-power applications. Resistance to static noise is one of the key parameters of the memory style, as it affects tolerance when reading and writing. SNM refers to the limiting voltages of a chemical metal compound (NMOS) based semiconductor as well as a metal oxide positive (PMOS) semiconductor of an SRAM cell. A high noise margin in reading and writing is additionally one amongst the main challenges in planning static random access memory. The memory voltage was calculated for a 6T SRAM cell for high speed applications [8]. With the reduction in feature size, the stability of static RAM has become a significant concern for future technologies. This crucial drawback are often resolved by employing a distinct and extremely stable bit-line SRAM cell, however up the time interval becomes crucial as a result of the differential sense amplifier can't be used for the read operation bit line. Sil et. al. proposed a new pseudo-differential single ended current sensing amplifier. they have a tendency to show that this style can give performance kind of like that of the standard current-mode differential amplifier while not mistreatment the double-bit line for read operations. The overall delivery time of the proposed single-ended design is 60% lower than the typical single-end design with 90 nm CMOS technology [9]. The 6-transistor cell (6T) which uses a pair of cross-coupled inverters is the most commonly used bit cell in today's SRAM projects [10].

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III. CONVENTIONAL 6T TRANSISTORS SRAM

The SRAM cell is symmetrically designed, however the dimensions of the transistors should be correct in order that the browse and write operations are correct. The performance needed for reading and writing stability should be achieved with tokenism area. The reading is performed with an adequate ratio relationship between pull down (PD) and pass gate (PG) transistors. Additionally, the soundness of the writing is confirmed by the proper relationship between gate transistors and elevation (PU) [11]. Typical cell 6T contains 2 CMOS adapters within the series. The output of the corresponding electrical converter is connected as input to a different inverter. Cell SRAM 6T is run throughout the whole write method, BL (bit line) at "1" or is reduced to "0" looking on the record, and BLB (linear bit line) is loaded additionally to BL. [12].

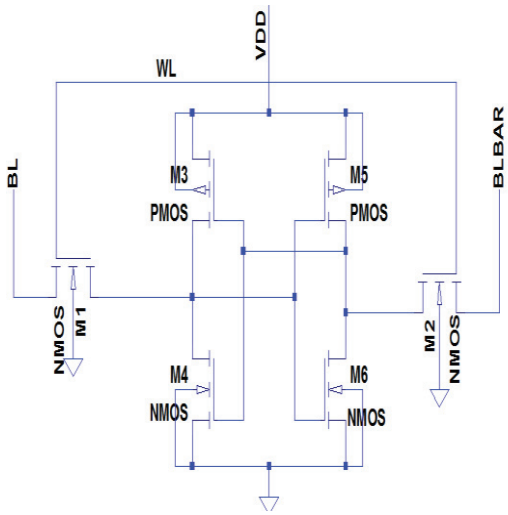

Fig. 1. Basic Circuit Diagram of 6T SRAM Cell

Fig 1 shows the actual SRAM architecture built on CMOS adapters. It consists of two inverted back-to-back couplers A and B, two transistors to reach M1 and M2. An access transistor is connected between the inverter and the BL and BLB bit lines, and their gates are connected to WL. The access transistor allows writing and reading across the word line and can be stopped while stopped. The port itself is used for reading and writing. In order to ensure that the cell operates, it is necessary to properly design the transistor. The SRAM cell can store data bits. The SRAM comprises two connected duplexers and two access transistors. The access transistor is used for writing and reading access to the cell. The SRAM cell provides the following basic properties.

- **Retention:** An SRAM cell will retain the information indefinitely whereas it's activated.
- **Read:** SRAM cells will connect data. This method doesn't have an effect on the information. In different words, the reading method isn't damaging.
- **Write:** SRAM information is outlined for any binary worth, despite its original information:

IV. PROPOSED SRAM CELL

Evaluate the expected SRAM cell impact on energy dissipation throughout the writing method. The provision voltage of the planned SRAM cell is 1V for various frequencies.VS1 and VS2 were taken during the simulation at 0.5 volts. These simulation results are compared with a standard SRAM 6T cell. The projected SRAM cell is shown in Fig 2. The projected SRAM cell is sculptural at completely different frequencies of 500Hz, 1GHz and 2GHz severally. Simulation results for frequencies of 500MHz, 1GHz and 2GHz are illustrated in Fig 3, 4 and 5 on an individual basis. Fig. 3, 4 and 5 show that the charging and discharging time of bits and bit lines has been improved for higher in operation frequency. Finally, we have a tendency to tend to calculate the dissipation of capability within the SRAM 500MHz, 1GHz and 2 of GHz SRAM cells, and compare these results with those obtained employing a typical SRAM 6-T cell.

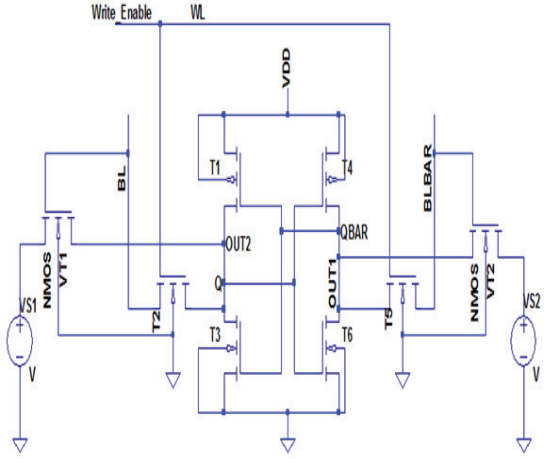

Fig. 2. Proposed SRAM Cell

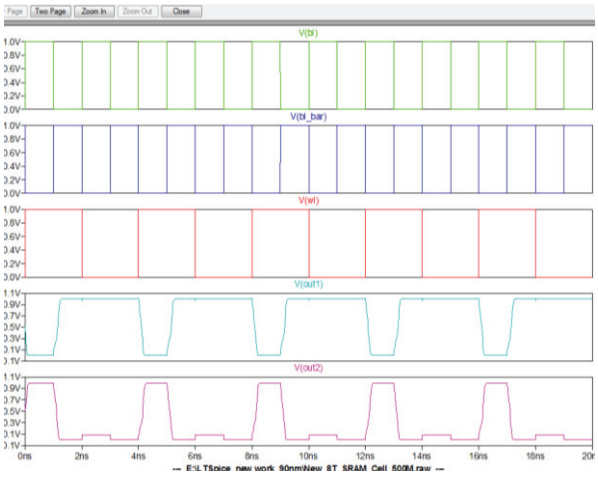

Fig. 3. Proposed SRAM cell for 500MHz

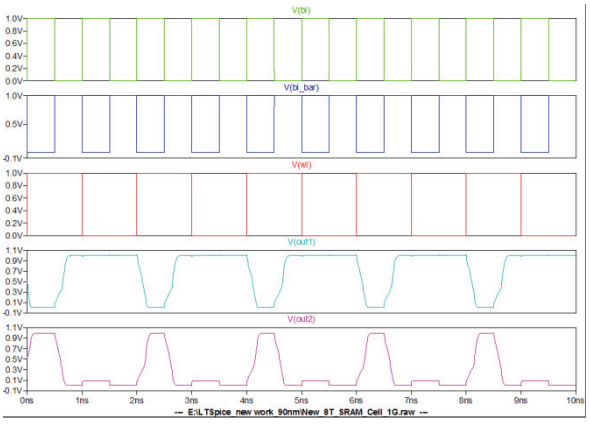

Fig. 4. Proposed SRAM cell for 1GHz

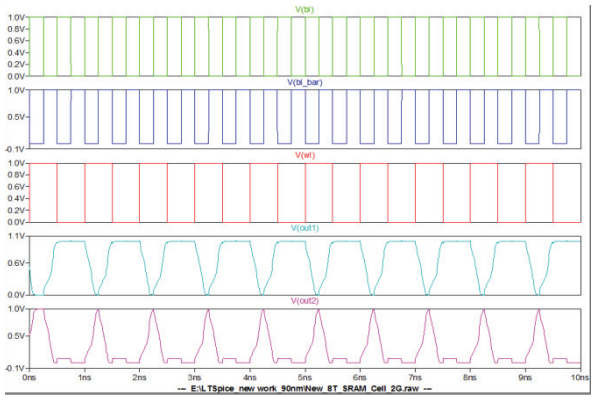

Fig. 5. Proposed SRAM cell for 2GHz

The width of the used transistor in proposed SRAM cell is shown in the table 1.

TABLE I. WIDTH USED IN THE PROPOSED MODEL FOR SIMULATION

Transistors	Widths(nm)
T1	175
T2	115
T3	500
T4	175
T5	115
T6	500

Table 2 shows a comparison of the spread power between a typical SRAM and, consequently, the projected model is shown in Table 2. This shows that when we tend to multiply the operative frequency of a customary SRAM cell, the ability dissipation is nearly doubled, however within the case of the projected power dissipation, the SRAM cell is concerning the dimensions and nearly constant at completely different frequencies like a traditional SRAM cell. it's thus clear from the results that the projected CMOS based SRAM style approach is appropriate for high-speed VLSI styles.

TABLE II. COMPARATIVE ANALYSIS OF POWER DISSIPATION BETWEEN CONVENTIONAL AND PROPOSED SRAM CELL

Operating frequency	Power Dissipation in 6T SRAM cell(μW)	Power Dissipation in Proposed SRAM cell(nW)
500MHz	4.890	606.519
1GHz	8.002	606.519
2GHz	11.979	606.519

In the projected SRAM cell, the values of interference voltage are raised by bit line, word line (WL) and output relative to the traditional SRAM cell, however these values are often controlled by size, acceptable width (W) and length (L) of the transistor.

V. CONCLUSION

There are two main styles of power dissipation wherever power dissipation has become a heavy downside of high-speed VLSI comes. In this paper, we have a tendency to propose a replacement method of an occasional power SRAM cell using the voltage mode methodology. This planned SRAM cell has 2 voltage sources that are wont to cut back the output voltage oscillation throughout the switch activity. The decrease in voltage oscillation has consequences of the reduction of power dissipation. The dispersion of the projected new SRAM cell is much stable for top speed operations. Due to the high number of transistors and regions compared to the traditional SRAM 6AM cell, this defect can be easily eliminated from very low energy consumption of a very high frequency. The planned SRAM is often wont to offer low-power solutions, such as laptops, smart phones, and programmable logic devices for high-speed devices.

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