Design of a wide tuning range VCO using an active inductor

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***Abstract*—This paper presents a wide tuning range CMOS voltage controlled oscillator suitable for radio frequency operation. The major advantage of this structure is the absence of on-chip inductor, thus reducing significantly the chip area. Measurements results using a $0.35\mu\mathrm{m}$ CMOS process from AMS have shown a wide tuning range of 84% of the $915\mathrm{MHz}$ central frequency and a phase noise around $-90\mathrm{dB}c/\mathrm{Hz}$ at $500\mathrm{kHz}$ offset from the carrier. The power consumption is reduced to less than $10\mathrm{mW}$ from a $3.3\mathrm{V}$ supply.**

I. Introduction

Voltage Controlled Oscillator (VCO) is an essential building block for Radio Frequency receivers. Ideally, a VCO provides a high stable frequency with a minimal power consumption. LC-tank VCOs, in which the frequency is determined by a passive tank circuit, offer the best performances in terms of phase noise. Although the tuning range of this kind of oscillator is relatively low (around 10% to 20%), phase noise below $-120\mathrm{dB}c/\mathrm{Hz}$ at $2.45\mathrm{GHz}$ can be achieved using this architecture [1], [2]. However, on-chip inductors exhibit poor performances at high frequency without active compensation. In addition, the number of inductors, very area-consuming, must be restricted in low-cost applications.

Using active inductors seems to be a good compromise. The global architecture remains the same and high quality factors are achievable even with a low supply voltage, minimizing the total consumption. Although the use of active inductors is known to degrade the phase noise of the VCO, it is still appropriate for many low-cost applications and can be improved with a proper design.

This paper presents a new VCO derived from the active inductor presented in Figure 1 [3]. Like in classical LC tank VCO, a negative resistance is used to compensate the losses of the inductors. The frequency is tuned by the value of the active inductor, controlled by the bias current.

II. Active Inductor Topology

A. Gyrator Topology

Figure 2 presents the traditional gyrator topology based on operational transconductance amplifiers (OTA).

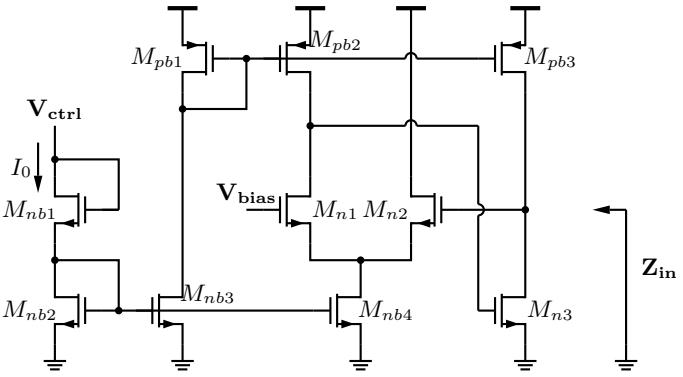

Figure 1. Active inductor topology

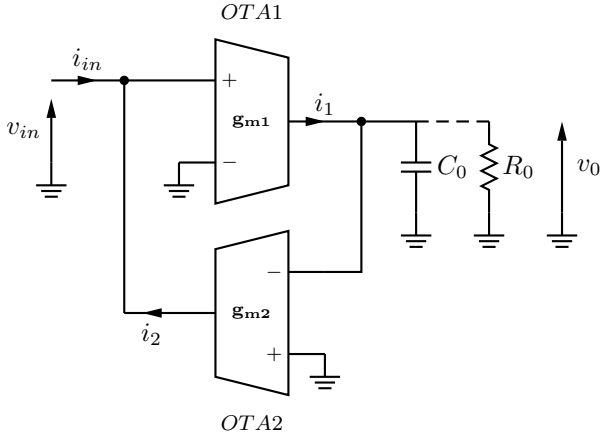

Figure 2. OTA-based gyrator

Considering ideal OTAs, this leads to an equivalent impedance at node in given by (1):

$$Z_{in} = \frac{v_{in}}{i_{in}} = jL_{eq}\omega = j\frac{C_0}{g_{m1}g_{m2}}\omega \tag{1}$$

If a parasitic resistance R_0 is present in parallel with C_0, which is usually the case in practical implementations, a parasitic resistance is introduced in series with L_{eq}:

$$r_{eq} = \frac{1}{g_{m1}g_{m2}R_0} \tag{2}$$

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B. Gyrator-type Active Inductor

The active inductor that composes the VCO is presented in Figure 1. This gyrator topology is the configuration that requires the less number of MOS transistors in the signal path (M_{n1}, M_{n2} and M_{n3}) and has been firstly introduced in [4]. This configuration has been modified so that the transistors in the signal path are all NMOS. Table I gives the sizes of the transistors that compose this inductor.

Four transistors, not represented in Figure 1, create the voltage reference at the gate of M_{n1}.

Table I
SIZE OF THE TRANSISTORS

Transistors	Type	Width (µm)	Length (µm)
M_{n1}, M_{n2}	nmos4	30	0.35
M_{n3}	nmos4	15	0.35
M_{nb1}, M_{nb2}, M_{nb3}	nmos4	10	0.35
M_{nb4}	nmos4	20	0.35
M_{pb1}, M_{pb2}	pmos4	5	2
M_{pb3}	pmos4	15	2

The first OTA is simulated by the differential pair M_{n1} and M_{n2}, the second OTA is obtained from the simple transistor M_{n3}. The total effective capacitance C_0 is the sum of all parasitic capacitances at the gate of M_{n3}:

$$C_0 = C_{gsn3} + C_{dbpb2} + C_{dbn1} \tag{3}$$

The parasitic resistance R_0, responsible for the appearance of r_{eq} in Figure 3 is given by:

$$R_0 = R_{dsn1}//R_{dspb2} \tag{4}$$

The equivalent impedance at node in is then shown in Figure 3:

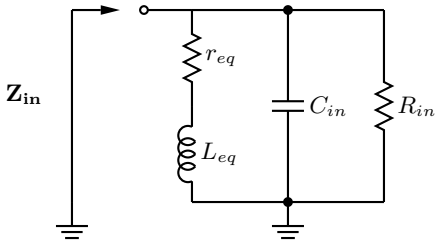

Figure 3. Real simulated inductance

From the small signal analysis of the circuit in Figure 1 we obtain:

$$L_{eq} = \frac{C_0}{g_{m1}g_{m2}} \tag{5}$$

$$R_{in} = R_{dsn3}//R_{dspb3} \tag{6}$$

$$C_{in} = C_{gsn2} + C_{dbn1} + C_{dbpb2} \tag{7}$$

$$r_{eq} = \frac{1}{g_{m1}g_{m2}R_0} \tag{8}$$

In these equations, g_{m1} is the equivalent transconductance of the differential pair, and $g_{m2} = g_{mn3}$ the transconductance of transistor M_{n3}. C_{gsi}, R_{dsi}, and C_{dbi} are respectively the parasitic gate-source capacitance, the parasitic output resistance of transistor, and the parasitic drain-bulk capacitance of transistor i.

We have neglected here the gate-source capacitance C_{gsn1} of the transistor M_{n1} since it introduces a high frequency pole at $\omega = 2C_{gsn1}/g_{mn1}$.

The quality factor of the active inductor is then given by:

$$Q_L = R_0 C_0 \omega \tag{9}$$

The quality factor being proportional to the high output resistance, this topology presents a high quality factor without any increase of the power consumption.

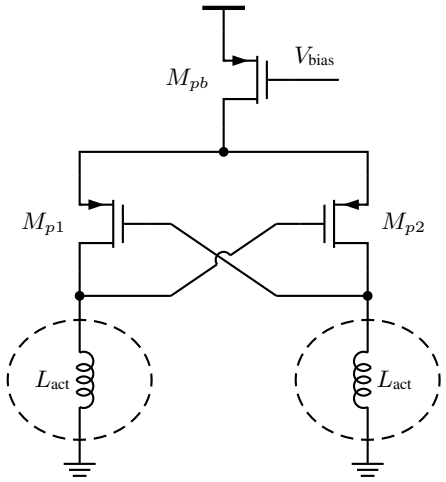

Figure 4. Proposed simplified VCO

III. PROPOSED VCO

The proposed VCO is presented in Figure 4. Here, the active inductor described in section II is duplicated to ensure a pseudo-differential operation, which suppresses even harmonics and reduces the noise. M_{p1} and M_{p2} form a positive feedback loop resulting in an active negative resistance used to compensate the losses of the simulated inductances. The total parasitical capacitance of the negative inductance only increases C_{in} by one C_{gs}. The total oscillation frequency is then given by:

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C_{tot}}} \tag{10}$$

Where $C_{tot} = C_{in} + C_{gsp}$.

The phase noise of this active inductor is given by :

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{max}^2\Delta\omega^2}\right] \tag{11}$$

In this equation, Γ_{rms} is the Impulse Sensitivity Function (ISF) of the oscillator. The total output noise $\frac{\overline{i_n^2}}{\Delta f}$ is simply the sum of the current noise of the active part and the negative resistor.

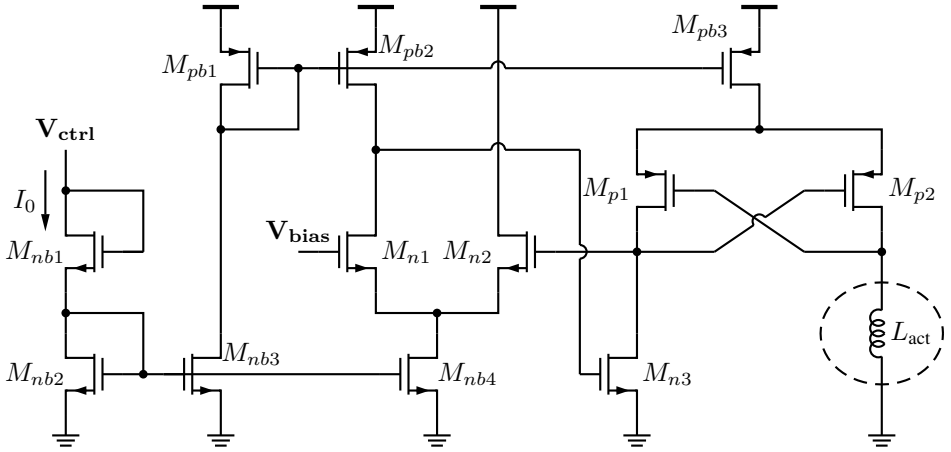

Figure 5. Half circuit of the complete VCO

To calculate the noise of the active part, we use the following noise model for the transistors:

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_{ds} + 4KT\delta g_m \tag{12}$$

where g_{ds} and g_m are the output conductance and transconductance of the transistor. The parameters $\gamma = 2$ and $\delta = 4$ take into account the short channel effects.

To reduce the phase noise at one input, we need to reduce g_{mn1}. However, this would reduce the oscillation frequency. Another option is to increase the gyrator capacitance, but that also reduces the frequency.

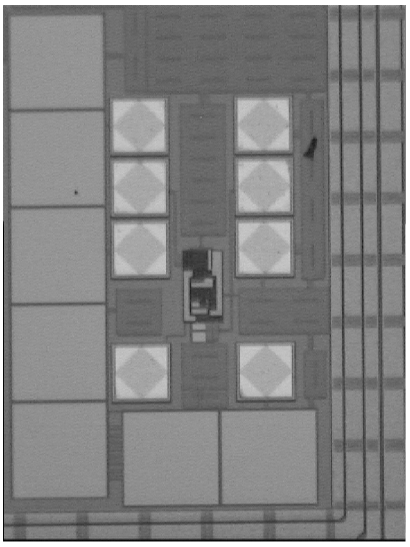

Figure 6. Photograph of the circuit used for measurements

IV. Experimental results

Figure 6 shows a picture of the circuit we used to get our measurement results. The pads and coupling capacitors are responsible for most of the surface used. The intrinsic area of this VCO is $80\mu\text{m} \times 40\mu\text{m}$.

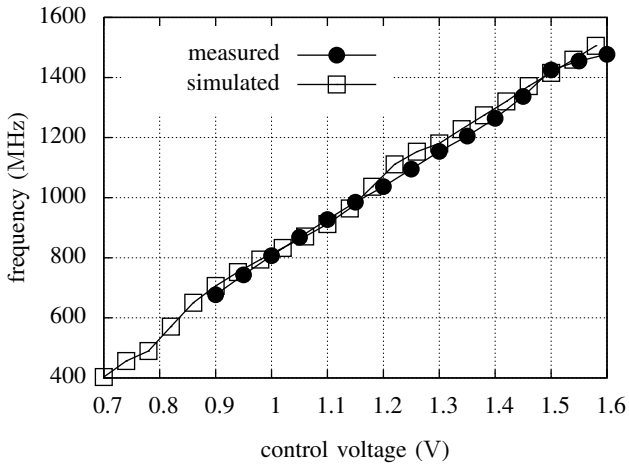

Figure 7. Simulated and measured oscillation frequency

Compared to a classical LC VCO at the same frequency, the proposed VCO occupies about 5 times less silicon area.

Figure 7 shows the oscillation frequency against the control voltage. The experimental frequency is close to the one given by post-layout simulations. The tuning frequency ranges from 680MHz to 1450MHz as the control voltage increases, allowing us to control precisely the operating frequency. Assuming 915MHz as the central frequency, that gives a measured tuning range $\Delta f/\Delta f_0$ of 84% for the proposed VCO. The measured gain is high : $K_{VCO} = 1100\text{MHz/V}$. Having such a high tuning range with this VCO is very important since this kind of circuit is strongly temperature dependent. Ensuring the correct operating frequency when used in a PLL for example requires a wide control to compensate the large temperature variations without the need of an additional PTAT.

A compromise between oscillation frequeny and phase noise has been obtained by simulation.

The phase noise of this VCO remains always better than $-87dBc/Hz$ at 500kHz from the carrier. Although it cannot be compared to the phase noise resulting from passive LC-tank

VCOs, this value can be compared with previous published work [5], [6].

For example, Figure 8 shows the measured phase noise of the VCO for a control voltage of 0.8V.

The total consumption of the proposed oscillator is less than $10.5\mathrm{mW}$ under $3.3\mathrm{V}$ supply voltage.

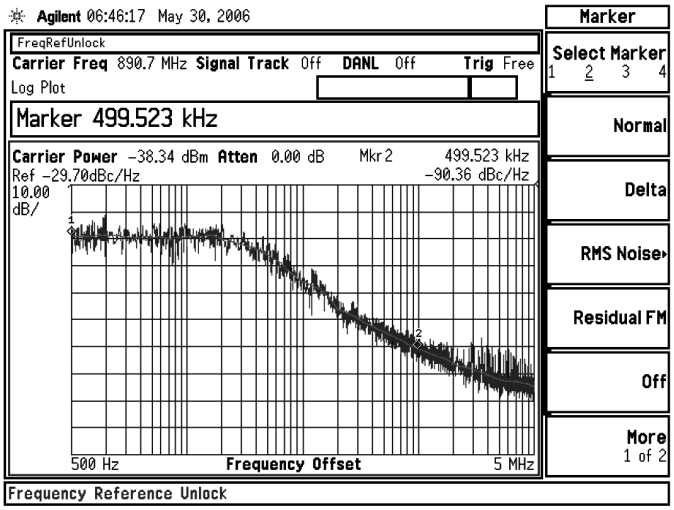

Figure 8. phase noise of the VCO for $V_{cont} = 0.8$

V. Conclusion

A wide tuning range voltage controlled oscillator using an active inductor has been described. The absence of on-chip inductors makes this circuit appropriate for on-chip applications. Simulations and measurements have confirmed the performances of this topology: wide tuning-range, low-power operation, and acceptable phase-noise.

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