Design of Low Voltage OTA for Bio-medical Application

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***Abstract*— This paper deals with the design of a low power signal conditioning circuit for use in biomedical applications. The signal conditioning circuit constitutes an opamp serving as a pre-amplifier and a low-pass filter for rejecting higher frequency components which are uncharacteristic of bio-medical applications. The Operational Transconductance Amplifier (OTA) design is done using UMC 180nm CMOS technology on the cadence virtuoso platform. The design is presented in terms of schematics and transistor dimensions. All relevant simulations is performed using spectre simulator at 1V power supply. The OTA's performance satisfies the required parameter for its implementation in biomedical portable devices. Corner analysis for gain and phase response have been performed at FF and SS corners for temperatures 100^0C and 0^0C respectively.**

Keywords*— biomedical; low power; operational transconductance amplifier; pre-amplifier; signal conditioning.

I. INTRODUCTION

There is an increasing trend in several biomedical applications such as pulse-oximetry, ECG, PCG, EEG, neural recording, temperature sensing, and blood pressure for signals to be sensed in small portable wireless devices, so, low-voltage supply operation is an important design issue [1]. The biomedical signals have a weak amplitude and low frequency, it always has been a challenge for biomedical electronic system to detect such signals. The recording electrodes might pick up other unneeded interference. However, the biomedical electronics might be unable to detect small biomedical signals. Therefore, we need a high gain, accurate, and high CMRR amplifier to reduce the common mode noise and to amplify the biomedical signal only.

In [2] authors has published a review report on ultralow power electronics and has pointed that sub-Vt operation is usually sufficient for biomedical application. Similarly, in [3] the authors has reviewed three characteristics namely low power consumption, low cutoff frequency and low input-referred noise for processing physiological signals. In-addition to this, the authors has also discussed the techniques to achieve the bove mentioned characteristics. In [4], the authors has designed an opamp using current-driven bulk techniques. Though the power consumption is high, it is a good technique for reducing the threshold voltage. Similarly, in [5], the authors has proposed an opamp using native NMOS transistor. Transistors in which channel is formed even when V_{GS} is zero are called native transistors. In [6] [7], the authors has designed bulk-input OTA, though it is a good techniques for low power operation but when compared to gate driven techniques it has more drawbacks.

Since, the relevant frequency range is till 250 Hz and more significantly around 100Hz for ECG signals, to eliminate noise at higher frequencies we use a low pass filter of cut-off frequency 100Hz. Based on the literature survey we adopted gate-driven MOSFET'S technique with PMOS input transistors working in weak-inversion region [8]. The transistors operating in weak-inversion region has higher trans-conductance which ultimately contributes to larger gain. The only major disadvantage is that the frequency response might not be well suited for high frequency operation, which can be neglected due to the fact that all the biomedical applications covered by this particular system have low frequency ranges (typically within 1kHz).

II. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER DESIGN

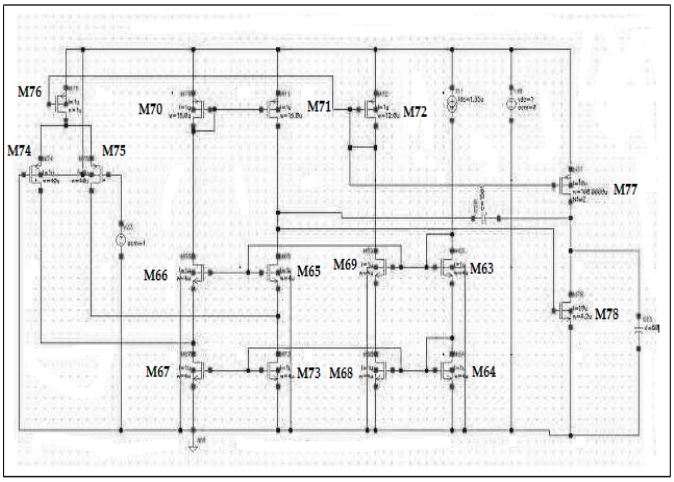

Fig.1 OTA Design

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The proposed OTA in our design contains two stages. A configuration similar to classical folded cascode was chosen for the first stage and a CSA like for the output stage. The whole circuit is shown in fig.1

A. First OTA stage

The main difference between the classical FC configuration and the proposed configuration is that the former has a stack of 4 transistors at its output, to obtain a high output resistance. The above OTA figure has a stack of 3 transistors. Assuming that all the devices are working in saturation ($V_{DSsat} \geq 0.1V$), and using 4 transistors at ultralow voltage supply produce an extremely reduced output swing. Hence, to increase the output swing and have relatively higher gains, 3 transistors are stacked. Nevertheless, an extra stage is needed to obtain better output swing.

A differential PMOS pair is used as input (M74 and M75), the bulks of the transistors are forward biased (tied to *VDD*) to reduce the V_{TH} and increase the inversion level. To have input transistors on the input dc level can be even as low as zero. Since, in sub-threshold region of operation we get low circuit speed, low power and high transconductance efficiency the input differential pairs are operated in sub-threshold region.

B. Output OTA stage Design

A second stage (M77, M78) is in cascade with the first stage and is used to achieve higher gains while maximizing the output swing. Table I shows the aspect ratio of all the transistors, their overdrive voltages, gm/Id and region of operation.

TABLE I. TRANSISTORS ASPECT RATIOS AND REGION OF OPERATIONS

Transistor's name	***W/L***	***Vov (in mV)***	G_m/I_D	***Region of operation***
M74,M75	40u/1u	179.7	27.12	Weak Inversion
M76	1u/1u	-1.5	27.12	Saturation
M70,M71	15u/1u	-4.8	27.10	Saturation
M66,M65	4u/1u	1.1	19.89	Saturation
M67,M73	4u/1u	1.9	21.53	Saturation
M72	12u/1u	-17.3	20	Saturation
M69.M63	4u/1u	3	21.38	Saturation
M68,M64	4u/1u	1.9	21.21	Saturation
M77	100u/10u	-49.8	21.21	Saturation
M78	4.2/10u	184.6	17.6	Saturation

III. SIMULATION

For the simulation of the OTA, BSIM3 models of 180nm CMOS process using the Cadence design environment. The simulation was done at all three corners namely TT, FF, and SS for gain and phase response. Input common mode range, output swing, power dissipation and input referred noise was also found under typical condition. The output signal displays a good phase margin. All the simulations were obtained using the Spectre simulator.

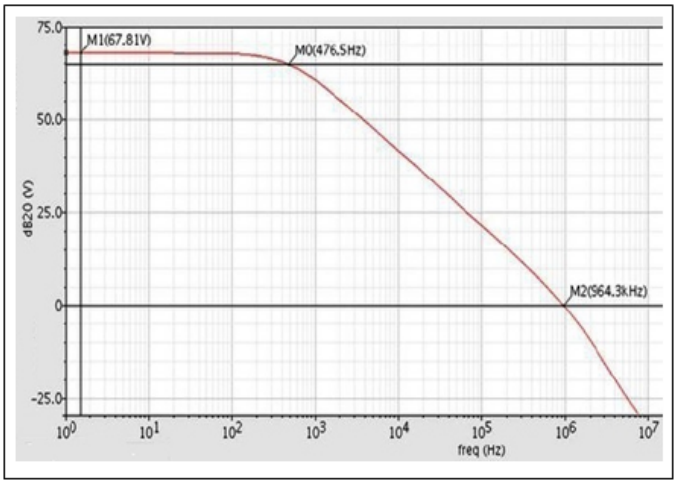

Fig. 2 Gain plot at typical conditions

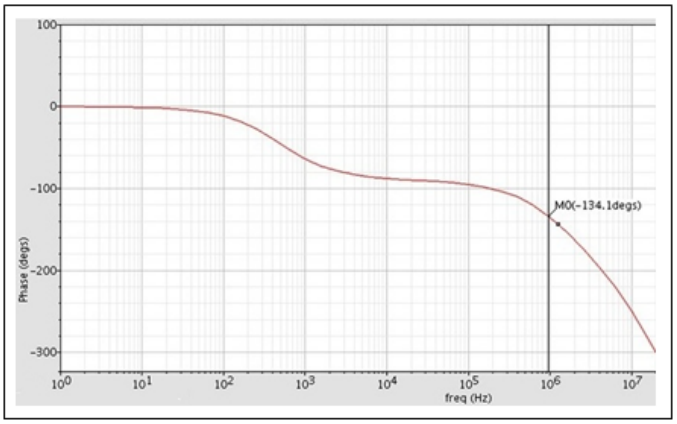

Fig. 3 Phase plot at typical conditions

As shown in fig.2 and fig.3 the DC gain achieved is 67.81 dB, 3-dB frequency is 476.5 Hz and the unity gain bandwidth is 964.3k Hz, which is also the gain crossover frequency. From the phase response and gain crossover frequency the phase margin is found to be 45.9 degrees. The circuit dissipates 7.243µW and has a high CMRR at low frequency.

The expression for low frequency dc gain for stage 1 and stage 2 are given as;

$$A_{v1} = -G_{m1}R_{out1} \quad (1)$$

Where,

$G_{m1} \approx g_{m74,75}$

$R_{out1} \approx [r_{o71} // \{ r_{o65} + (r_{o73}//r_{o75}) + (g_{m65}+g_{mb65})r_{o65}(r_{o73}//r_{o75})]$

The gain of the second stage is given by;

$$A_{v2} = -G_{m2}R_{out2} \quad (2)$$

Where,

$G_{m2} \approx g_{m78}$

$R_{out2} \approx r_{o77} // r_{o78}$

The total gain of the amplifier is the product of A_{v1} and A_{v2}.

$$Av = A_{v1} \times A_{v2} \quad (3)$$

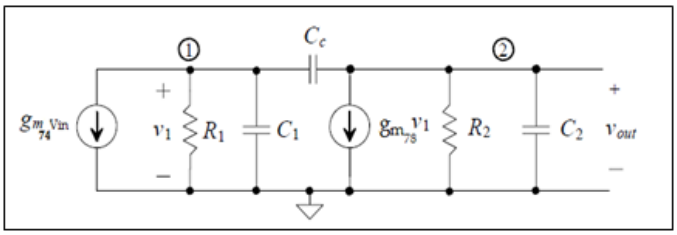

Fig.4 Circuit for calculating the transfer function.

The small signal ac model for the OTA design is shown in fig. 2. R1and R2 are the output resistance of stage 1 and stage 2 respectively, and C1 and C2 are the total lumped capacitances. Cc is the miller capacitance having value of 150fF. The transfer function for the above OTA model is given by;

$$\frac{Vout(s)}{Vin(s)} = g_{m,74}R_1 g_{m,78}R_2 \frac{\left(1-\frac{s}{z_1}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} \quad (4)$$

Where,

$$z_1 = \frac{g_{m78}}{Cc}$$

$$p_1 = -\frac{1}{g_{m78}R_1R_2Cc} \quad (5)$$

$$p_2 = -\frac{g_{m78}}{C_1 + C_2}$$

$$UGB = \frac{g_{m74}}{Cc}$$

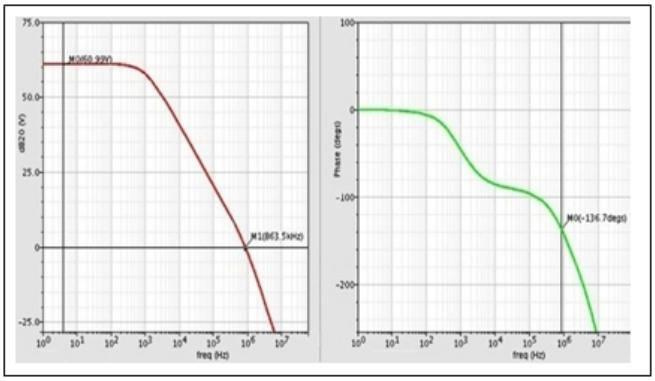

Fig. 5 Gain and Phase at FF Corner

Fig. 5 and fig. 6 shows the gain and phase response at FF and SS corner respectively. The gain is 60.99dB and phase is 43.3 degrees at temperature 100^0C was achieved, whereas, at SS corner gain is 59.02dB and phase is 56.1 degrees at temperature 0^0C. Thus, not much variation has been seen in the corners.

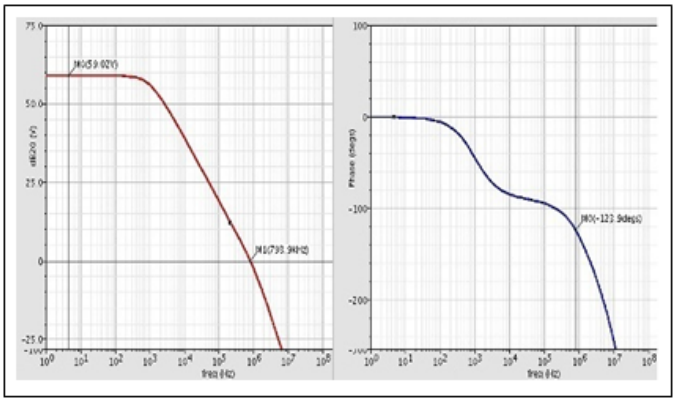

Fig. 6 Gain and Phase at SS Corner

The circuit has a very high input common mode range (ICMR) due to pmos input transistors. The input PMOS transistors are in weak inversion region, so, $V_{SG74,75}$ should be less than or equal to $|V_{TP}|$. For high input CM, the transistor M76 should remain in saturation and for low input CM, the transistors M66,65 should remain in saturation. Since, the inputs are PMOS transistors the minimum input CM can go as low as 0V. The expression for ICMR are shown below;

$$V_{icm} < V_{bias76} - V_{SG74} + |V_{TP}| \quad (6)$$
$$V_{icm} > V_{bias66} - V_{GS66} - |V_{TP}| + V_{SD74}$$

Fig. 7 shows the ICMR plot. It is estimated from the straight line corresponding to the above simulation to be 0 mV to 854.3 mV.

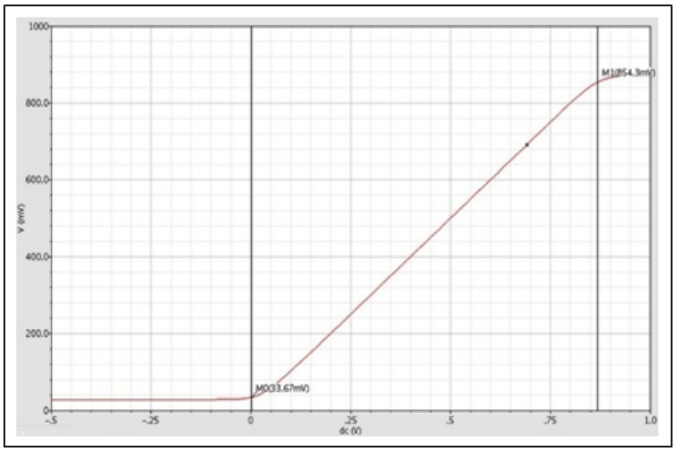

Fig. 7 Input common mode range (ICMR)

With the use of CSA as the output stage there is an increase in the lower end of the swing. For the first stage (folded cascode) the lower end of the swing is given by $V_{OV73} + V_{OV65}$ and the upper end by $V_{DD} - |V_{OV71}|$. The overall swing of the OTA is $V_{DD} - V_{OV77} - V_{OV78}$. So, there is an increase of output swing by one overdrive voltage.

The output swing has also been calculated using the simulation. Fig. 8 shows the output swing and is calculated to be 795.7 mV. The use of Common Source Amplifier as the output stage helps to improve the swing considerably.

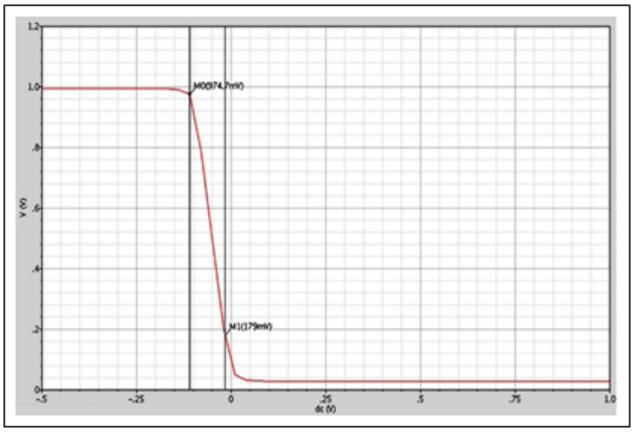

Fig. 8 Output swing

Slew rate is calculated as dV_{out} / dt . Hence from fig. 9 the slew rate is 0.052 V/ µs . The noise behavior is shown in fig. 10, where the flicker noise decreases from 105µV/$\sqrt{Hz}$ @ 1Hz to 17µV /$\sqrt{Hz}$ @ 100 Hz.

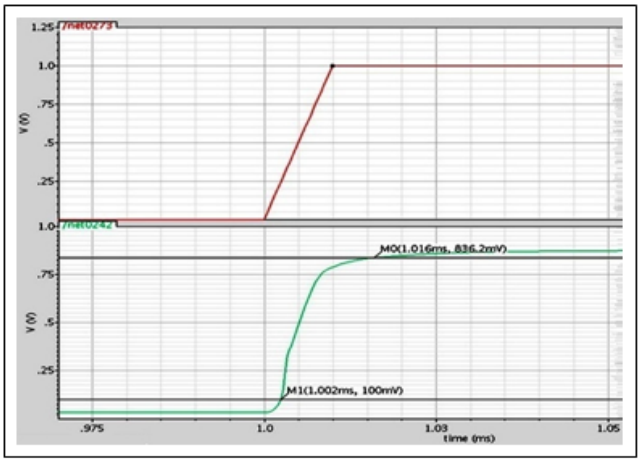

Fig.9 Slew rate

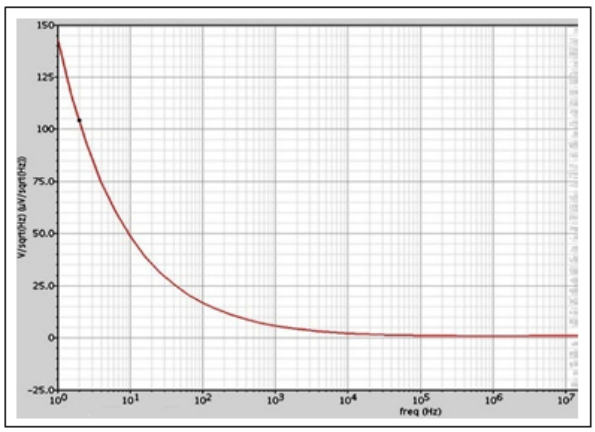

Fig. 10 Input referred noise

A summary of the simulation results are tabulated in table II. The OTA designed consumes 7.243µW power and has high open loop DC gain. The circuit gives a large gain bandwidth and high common mode rejection ratio (CMRR) of 104.95dB @ 10Hz.

TABLE II. SUMMARIZED RESULTS

Parameters	Values Obtained
Open loop Gain	67.81 dB
Gain Bandwidth	964.3 kHz
Phase Margin	45.9 degrees
CMRR @ 10 Hz	104.95 dB
Input Referred Noise	9 uV/sqrt(Hz)
Power Consumption	7.243 uW
ICMR	0-854.3 mV
Output Swing	795.7mV
Slew rate	0.052V / µs

Butterworth filters are termed maximally-flat-magnitude-response filters, optimized for gain flatness in the pass-band. The attenuation is –3 dB at the cut-off frequency. Above the cut-off frequency the attenuation is –20 dB/decade/order. The transient response of a Butterworth filter to a pulse input shows moderate overshoot and ringing. The gain response of the filter is shown in fig. 11 from which it can be observed that the pass band gain is 25.9 dB. The cutoff frequency of the filter is 100.4 Hz.

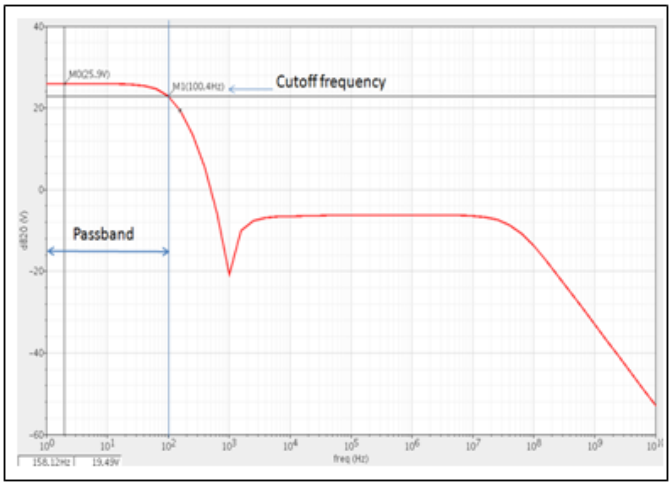

Fig.11 Gain Response of 2nd order butterworth filter.

From the fig. 11 the initial roll off rate is 40dB / decade which is characteristic of a second order filter. Pass band Ripple is zero owing to the fact that the filter designed is a Butterworth filter.

IV. CONCLUSION

The differential input single output OTA that operates with 1V power supply has been designed in this paper. The design

does not require special technology as all the transistors are gate driven. Using PMOS as the input transistors biased in sub-threshold/weak-inversion is more advantageous than using the bulk-driven or floating-gate techniques for biomedical applications. The OTA's performance satisfies the required parameters for its implementation in biomedical portable devices. The 2nd order Butterworth filter gives the optimum performance for a given application.

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