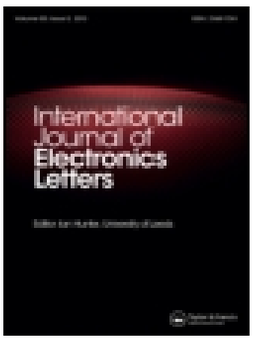

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Design of CMOS-based low-power high-frequency differential ring VCO

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ABSTRACT

An improved design of four-stage CMOS differential ring voltage-controlled oscillator (VCO) with high-output frequency, low phase noise, and low power consumption is proposed in this paper. A new differential delay cell has been used for differential ring VCO which utilises dual-delay-path topology to attain both high-output frequency and low phase noise. The simulation results have been obtained in TSMC 0.18-µm CMOS process with a supply voltage (V_{dd}) 1.8 V. The proposed design of VCO exhibits an output oscillation frequency range from 1.619 to 3.712 GHz. The power consumption for this frequency range varies from 4.628 to 10.545 mW with control voltage variation from 0.1 to 1.0 V. The proposed design occupies compact layout area of 0.207 mm^2 and achieves –89 dBc/Hz phase noise at 1 MHz offset from 3.712-GHz carrier frequency. Improved performance for this design has been achieved in terms of output oscillation frequency, phase noise, and power consumption.

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KEYWORDS
Differential delay cell; dual-delay-path topology; low phase noise; low power; phase-locked loop; VCO

1. Introduction

Ring voltage-controlled oscillator (VCO) is the essential block in phase-locked loops, clock generation, and data recovery circuits which has been widely used in modern communication systems (Haijun, Lingling, Xiaofei, & Liheng, 2012; Kumar, Arya, & Pandey, 2015; Rezayee & Martin, 2001). Ring VCO and LC tank VCO are the two categories of the VCO architectures which are extensively used in the design of a PLL system (Hsieh, Welch, & Sobelman, 2010; Kumar, 2016). A ring VCO has a number of delay cells, with the output of the last delay cell fed back to the input of the first delay cell. The delay cell in a ring VCO can be single-ended or differential. The design of single-ended ring VCO is very simple; it is a chain of inverters having an odd number of the delay cell. A single-ended rind VCO consumes very low power but it suffers from noise cancellation problem (Jalil, Reaz, & Ali, 2013). Differential delay cell is used to design ring VCO to improve this problem. Differential ring VCO design provides more flexibility in modulating the output frequency because it can have an odd or even number of the delay cells. A ring VCO with differential delay cell is used to reduce the substrate noise and power supply injected phase noise (Tao & Berroth, 2003). The major requirements

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for the design of differential ring VCO are large output frequency range and low phase noise. The phase noise expression for the CMOS differential ring oscillator is given as follows (Parvizi, Khodabakhsh, & Nabavi, 2008):

$$L_{\min}(\Delta f) = \frac{8}{3\eta} N \frac{kT}{P} \left(\frac{V_{dd}}{V_{cr}} + \frac{V_{dd}}{R_L I_{tail}} \right) \frac{f_0^2}{\Delta f^2} \tag{1}$$

where V_{dd} is the supply voltage, R_L is the load resistor, I_{tail} is the tail bias current, V_{cr} is the characteristic voltage of the device, f_{o} is the oscillation frequency and Δf is the frequency offset from the carrier, N is the number of stages, K is Boltzmann constant, T is absolute temperature, P is the power consumption and η is the proportional constant. The design of a ring VCO has a trade-off between its frequency range and phase noise (Li & O, 2005). With the increase in its gain, the output frequency increases and consequentially, the phase noise performance of the VCO degrades as per Equation (1). Due to their excellent phase noise performance, LC VCOs are generally used in wireless communication systems (Azqueta, Celma, & Aznar, 2011; Tiao & Sheu, 2010). The ring VCO has low power consumption compatible with digital CMOS processes and occupies small on die area and wide tuning range (Jin, 2014; Tu, Yeh, Tsai, & Wang, 2004; Zhang et al., 2014) as compared to the LC VCOs. A delay cell is the main module in a VCO and any improvement in its design will improve its overall performance, and hence a PLL system. In this paper, a differential ring VCO has been designed due to its better overall performance in terms of the high-output frequency, low power consumption, and low phase noise. A four-stage differential ring VCO with desired features using the improved design of differential delay cells has been proposed.

This paper is arranged as follows. Section 2 presents the architecture of a differential ring VCO with dual-delay-path topology with operation of conventional and proposed differential delay cell. Simulation results and design comparison with earlier reported VCOs are given in Section 3. Finally, Section 4 concludes the paper.

2. Design description of differential ring VCO circuit

2.1. *Architecture of differential ring VCO with dual-delay-path topology*

In a ring oscillator, only a V_{dd} is required to operate. For the fixed V_{dd}, the output oscillation frequency (f_o) of a ring VCO can be determined by a number of delay cells (N) connected in the closed loop and the propagation delay time (t_d) of each delay cell as shown in Figure 1. If N is fixed, the delay time of each cell is changed by applying the different control voltage, V_c at the control input of VCO. The output oscillation frequency of a differential ring oscillator can be expressed as follows (Sheu, Tiao, & Taso, 2011):

$$f_o = \frac{1}{2t_d N} \tag{2}$$

It is depicted from (2), the parameter that changes the output oscillation frequency is a propagation delay time of each delay cell and the number of stages. The output oscillation frequency of the ring VCO is limited because delay time cannot be lesser than that of a single inverter. To remove frequency limitation problem, a negative skewed

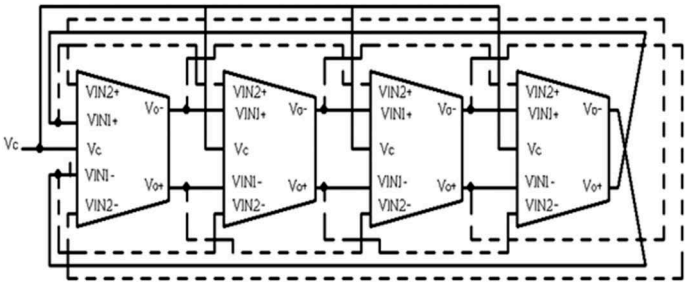

Figure 1. Four-stage differential ring VCO structure with dual-delay-path topology.

delay design is used (Park & Kim, 1999). The negative skewed delay path design reduces the delay time of a ring VCO below the delay time of a single inverter. The normal delay signal is connected to the input of NMOS transistor M_1 and M_2, whereas negative skewed signal is connected to PMOS transistor M_5 and M_6 is shown in Figures 2 and 3.

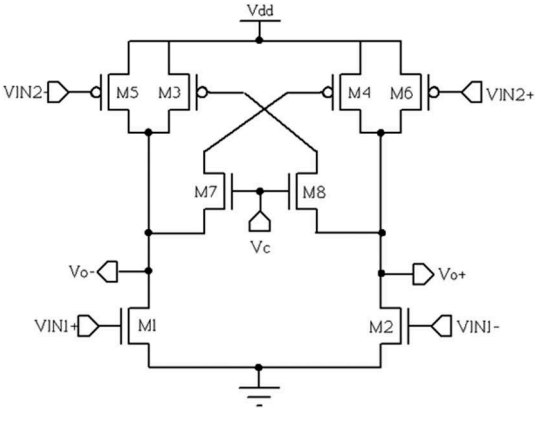

Figure 2. Conventional four input differential dual-delay cell.

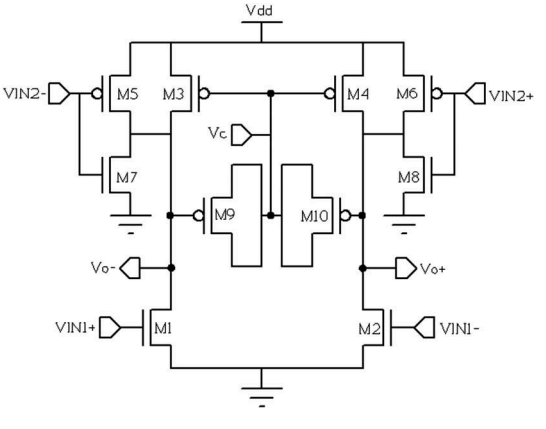

Figure 3. Four input proposed differential dual-delay cell.

Ring VCO structure with dual-delay-path enables the wider tuning range and higher the output oscillation frequency (Chen and Lee 2011; Kim, Kim, Lee, Han, & Lee, 2013; Ren, Emmert, & Siferd, 2011). The skewed signal is taken from outputs of two stages before the existing delay cell. The skewed signal improves the performance of PMOS transistor which is slower than NMOS transistor because it turns ON the PMOS transistor prematurely. This process reduces the rise time of the output signal resulting the higher output oscillation frequency. As skewed delay signal increases, the oscillation frequency as well as power consumption increases. Further, the increment in skewed signal decreases the speed and increase the power consumption of the ring VCO due to direct path exist between the power supply and ground. The skewed delay must be less as compared with the total period to obtain the higher oscillation frequency with lower power consumption. The skewed delay path is shown by a dotted line and normal delay path is represented as a solid line in Figure 1. The power consumption of a differential ring VCO is given as follows (Parvizi et al., 2008):

$$P = NI_dV_{dd} \tag{3}$$

In order to satisfy the optimum performance of power consumption of ring VCO, the number of delay stages (N) can be elected. For a fixed V_{dd}, the number of delay stages increases, the current I_d to the entire delay stages should be decreased to satisfy the power requirement. The ring VCO circuit becomes vulnerable to noise as the level of current I_d turns out to be too low.

2.2. *Conventional delay cell*

The conventional four input differential dual-delay cell is shown in Figure 2. In this configuration, a differential input made up of two NMOS transistors M_1 and M_2 which act as primary inputs. A couple of PMOS load transistors M_3 and M_4 are used to comprise a CMOS latch block. The strength of CMOS latch block in the delay cell will affect the oscillation frequency. The cross-coupled NMOS transistor M_7 and M_8 are used to form the controlled block. They control the strength of the CMOS latch block. Two PMOS transistors M_5 and M_6 are connected to PMOS load transistors to acquire a negatively skewed signal. Transistors M_5 and M_6 is used to increase the output frequency of VCO.

2.3. *Proposed delay cell*

The design of four input proposed differential dual-delay cell is shown in Figure 3. In this configuration, $V_{\text{in1-}}$ and $V_{\text{in1+}}$ form the primary inputs. Two transistors M_3 and M_4 are used as a PMOS load. The oscillation frequency can be modulated with the change in the control voltage (V_c), applied to the gate terminal of load transistor M_3 and M_4 and drain source terminal of M_9 and M_{10} transistors are used as a varactor. With the decrease in control voltage, the value of resistance of M_3 and M_4 transistor and capacitance of M_9 and M_{10} transistor decreases. The time constant of differential dual-delay cell decreases, resulting in the higher output oscillation frequency. Conversely, if the control voltage is increased, the value of resistance of M_3 and M_4 transistor and capacitance of M_9 and M_{10} transistor increases. As a result, the frequency at the output terminal decreases. When the primary input signal $V_{\text{IN1+}}$ has a lower value than V_{THn}, then transistor M_1 turns off. Since input signal at transistor M_5 appears earlier than transistor M_1, as a result transistor

M_5 starts conducting. Therefore, the output terminal of the delay cell charges the lower to higher voltage and this process decrease the rise time at the output terminal. Two NMOS transistor M_7 and M_8 are attached with a pair of secondary input. These transistors predischarge the output terminal and also decreases the fall time of the output signal. The proposed VCO has higher output frequency due to predischarge operation. A couple of M_9 and M_{10} PMOS transistors connected in series used as a varactor at the output terminal of the dual-delay cell which enhances the tuning range. The aspect ratio of the MOS devices used in proposed design are given in Table 1.

Figure 4 shows the two PMOS transistor M_9 and M_{10} connected in series acting as a varactor. In this structure, the drain and source terminals are tied together to form one node of the capacitor and gate terminal as the other node. The device capacitance is equivalent to the series connection of gate oxide capacitance with depletion layer capacitance. The depletion layer capacitance depends on the gate voltage. The gate voltage of M_9 and M_{10} transistors is selected in such a way that these transistors operate in accumulation region (Andreani & Mattisson, 2000). As V_{gs} goes below $V_{THp,}$ a depletion layer is generated under the gate and generate depletion capacitance C_d. Therefore the overall capacitance decreases due to a series combination of C_{ox} and C_d. When V_c decreases, the value of capacitance decreases and obtained the maximum output oscillation frequency and vice versa.

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d}\frac{C_d C_{ox}}{C_d + C_{ox}} \tag{4}$$

$$C_{\min} = \frac{C_d + C_{ox}}{C_d C_{ox}} \tag{5}$$

$$C_{\min} = \frac{\varepsilon A}{d} = \frac{\varepsilon_o \varepsilon_r WL}{t_{ox}} = \frac{\varepsilon_{ox}}{t_{ox}} = C_{ox} WL \tag{6}$$

Table 1. Transistor size of MOS for proposed design.

Transistor name	Width/length ratio
M1, M2	$\frac{2}{0.18}, \frac{2}{0.18.}$
M3, M4	$\frac{4}{0.18}, \frac{4}{0.18}$
M5, M6	$\frac{4}{0.18}, \frac{4}{0.18}$
M7, M8	$\frac{1}{0.18}, \frac{1}{0.18}$
M9, M10	$\frac{1}{0.18}, \frac{1}{0.18}$

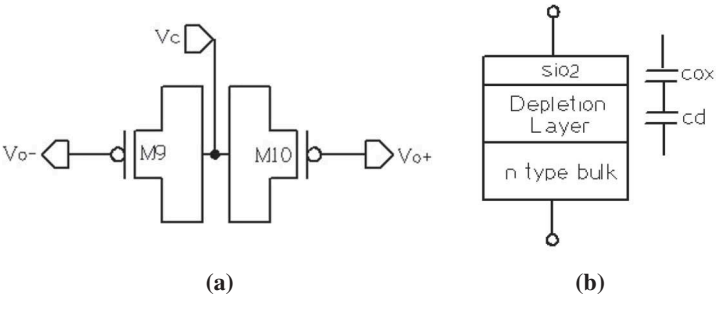

Figure 4. (a) PMOS varactor. (b) Cross-section of gate and depletion region.

3. Result and discussion

The four-stage differential ring VCO with a proposed four input differential dual-delay cell has been designed in TSMC 0.18-µm CMOS process. Table 2 shows the simulation results of proposed differential ring VCO. The output waveform of proposed ring VCO is shown in Figure 5. The proposed ring VCO demonstrate the output frequency range from 1.619 GHz to 3.712 GHz and power consumption variation in the range from 4.628 to 10.545 mW with the change in control voltage from 0.1 to 1 V while maintaining supply voltage at 1.8 V. The phase noise of the proposed VCO is −89dB/Hz @ 1-MHz offset from the 3.712-GHz carrier frequency as shown in Figure 6. The VCO performance may also be estimated by using the following figure of merit (FoM). The FoM is based on the single oscillation frequency is defined as follows (Azqueta et al., 2011):

$$FoM = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{P_{Diss(mW)}L(\Delta f)}\right] \tag{7}$$

Table 2. Results of VCO.

	Different values of supply voltage							
	V_{dd} = 1.8V		V_{dd} = 1.7V		V_{dd} = 1.6V		V_{dd} = 1.5V	
Control voltage (V)	Output frequency (GHz)	Power dissipation (mW)	Output frequency (GHz)	Power dissipation (mW)	Output frequency (GHz)	Power dissipation (mW)	Output frequency (GHz)	Power dissipation (mW)
0.1	3.712	10.545	3.540	8.657	3.341	6.980	3.108	5.509
0.2	3.269	9.855	3.106	7.966	2.902	6.297	2.650	4.871
0.3	2.965	9.054	2.762	7.172	2.539	5.519	2.300	4.293
0.4	2.650	8.175	2.448	6.334	2.230	4.733	1.997	3.375
0.5	2.351	7.312	2.177	5.542	1.976	4.020	1.776	2.746
0.6	2.138	6.565	1.959	4.886	1.783	3.460	1.590	2.283
0.7	1.946	5.912	1.795	4.335	1.635	3.014	1.457	1.948
0.8	1.806	5.364	1.667	3.897	1.514	2.691	1.356	1.758
0.9	1.709	4.931	1.582	3.582	1.439	2.516	1.29	1.748
1.0	1.619	4.628	1.505	3.413	1.386	2.512	1.205	1.705

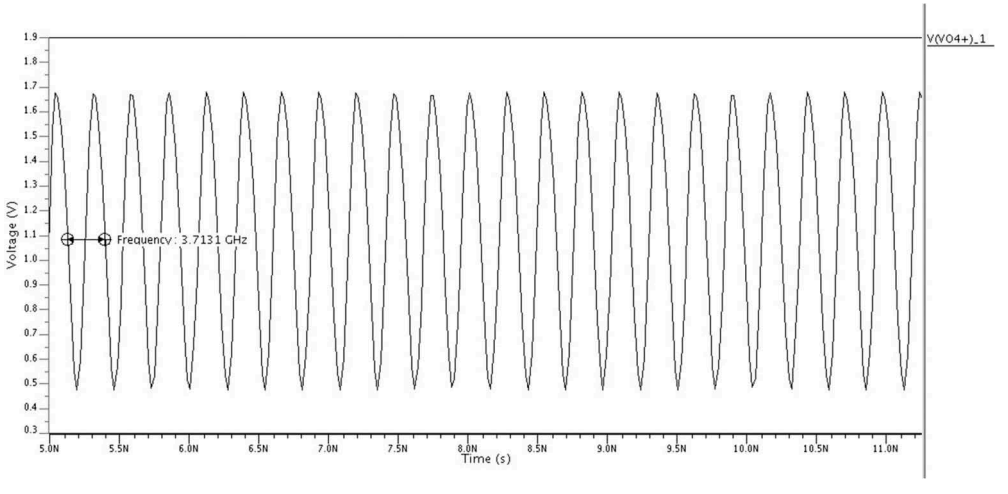

Figure 5. Output waveform of proposed VCO at V_{dd} = 1.8V and V_c = 0.1V.

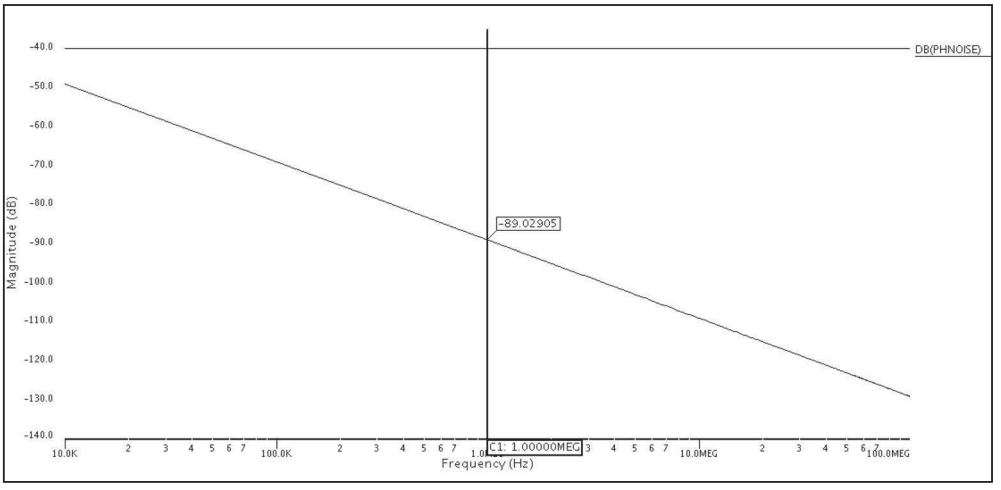

Figure 6. Phase noise of proposed differential ring VCO at 1-MHz offset.

where P_{Diss} is the power dissipation, f_o is the oscillation frequency and Δf is the frequency offset from the carrier. The FoM obtained for proposed VCO circuit is −150.19 dB_C/Hz. The layout of proposed ring VCO is shown in Figure 7 and it acquires area of 0.207 mm^2. The post layout VCO simulation shows output frequency range from 1.687 GHz to 3.622 GHz and consumes power of 10.96 mW. The proposed VCO has also been designed and simulated in TSMC 0.35-and 0.25-µm CMOS process with supply voltage 3.5 V and 2.5 V respectively. The VCO circuit with 0.35-µm CMOS process has tuning range from 1.328 to 2.001 GHz and consumes power 41.52 mW, while with 0.25-µm CMOS process VCO shows frequency variation from 1.704 to 2.536 GHz and consumes power 20.21 mW. A comparison analysis of power and tuning range of proposed design with existing VCOs is shown in Figures 8 and 9. VCO reported (Rezayee & Martin, 2001) has excellent tuning range but consumes huge power, while VCO circuit (Zhang et al., 2014) has small power consumption and less tuning range. The proposed design shows the improved power consumption and tuning range as compared to the existing design. The obtained results of proposed design with 0.35-, 0.25-, and 0.18-µm CMOS process are compared with previously reported designs of VCO as shown in Table 3.

4. Conclusion

The four-stage CMOS differential ring VCO with a proposed differential dual-delay cell has been designed in TSMC 0.18-µm CMOS process. The differential VCO utilises dual-delay-path topology to achieve high-output oscillation frequency. To enhance the output oscillation frequency of proposed differential dual-delay cell, two NMOS M_7 and M_8 transistors are attached with secondary input and two PMOS M_9 and M_{10} transistor is used as a varactor at the output terminal of the dual-delay cell to increase the tuning range. The four-stage differential ring VCO design oscillates from 1.619 GHz to 3.712 GHz and dissipates power from 4.628 mW to 10.545 mW with a variation of the control voltage from 0.1 V to 1.0 V. The phase noise of proposed differential ring VCO is – 89 dBc/Hz at 1 MHz

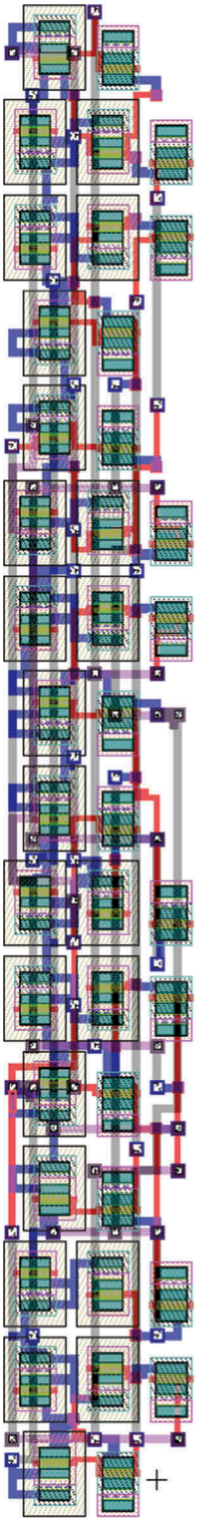

Figure 7. Layout of proposed differential ring VCO.

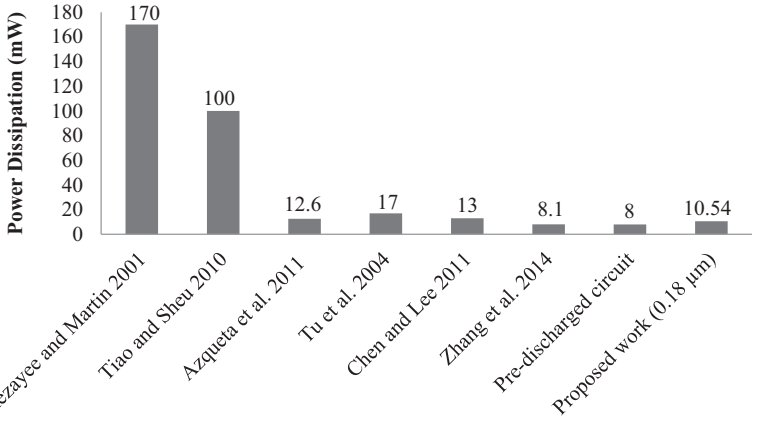

Figure 8. Comparative analysis of power dissipation of proposed VCO with existing VCOs.

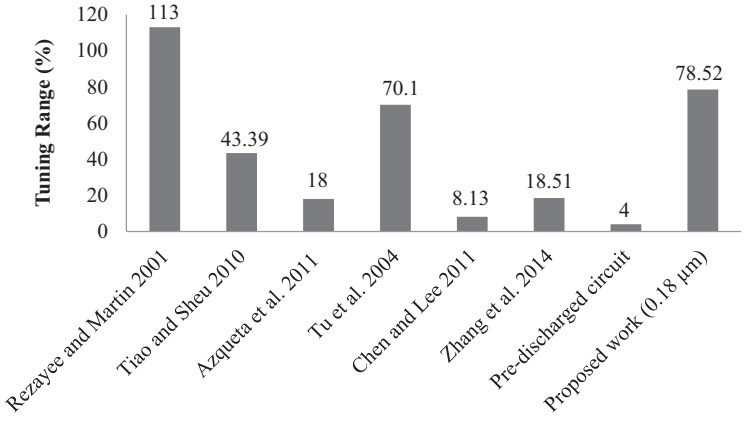

Figure 9. Comparison of tuning range of proposed VCO with existing VCOs.

Table 3. VCO performance comparisons.

References	Process (µm)	Supply (V)	Oscillation frequency (GHz)	Tuning range in % (GHz)	Control Voltage (V)	Power dissipation (mW)	Phase noise (dBc/Hz) @ 1MHz	FoM (dBc/Hz)
Rezayee and Martin (2001)	0.18	1.8	2.5–9.0	113	0V–0.9V	170	−82	−133.6
Tiao and Sheu (2010)	0.18	1.8	3.03–5.36	43.39	0V–1.8V	100	−107	−161.3
Azqueta et al. (2011)	0.18	1.8	–	18	−0.8V–0.2V	12.6	−91	−149.1
Tu et al. (2004)	0.18	1.8	2.5–5.2	70.1	−0.4V–0.4V	17	−90.1	−148.9
Chen and Lee (2011)	0.18	1.8	1.77–1.92	8.13	0V–1.8V	13	−102	–
Zhang et al. (2014)	0.18	1.8	4.9–5.9	18.51	0V–1.8V	8.1	−86.7	−149.7
Proposed work with pre-discharged circuit only	0.18	1.8	4.96–5.12	4	0.2–1	8	−85	−149.8
Proposed work	0.35	3.5	1.32–2.00	40.96	0.1V–1.0V	41.52	−79	−128.8
	0.25	2.5	1.70–2.53	39.33	0.1V–1.0V	20.21	−82	−137
	0.18	1.8	1.61–3.71	78.52	0.1V–1.0V	10.54	−89	−150.1

offset and FoM is −150.9 dB/Hz. The VCO design occupies the layout area of 0.207 mm^2. The proposed VCO result shows the improved performance in terms of the oscillation frequency, power consumption, and phase noise.

Disclosure statement

No potential conflict of interest was reported by the authors.

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