Received: 8 January 2018 | Revised: 24 October 2018 | Accepted: 28 October 2018

DOI: 10.1002/cta.2582

RESEARCH ARTICLE

WILEY

Design and analysis of differential ring voltage controlled oscillator for wide tuning range and low power applications

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Summary

Voltage-controlled oscillator (VCO) is the most basic component required for all wireless and communication systems. In this article, a four-stage differential ring VCO with two control voltages for wide tuning range is proposed. This VCO uses the dual-delay loop technique for high operation frequency. Also, a low-V_T NMOS transistor is used in series with pull down network of the proposed VCO delay cell to achieve low frequencies. Prelayout simulation of the proposed VCO is performed in 65-nm TSMC CMOS technology in Cadence software under 1.2-V supply voltage. The tuning range of the proposed VCO varies from 1 MHz to 13.8 GHz and has been improved by 19.77% compared to other works. The power consumption of this low power VCO is between 29.3 μW to 1.715 mW. The phase noise of the proposed circuit is −82.3 dBc/Hz at 1 MHz offset frequency and −106.9 dBc/Hz at 10 MHz offset frequency from 5.161 GHz center frequency, while its area is 102.457 μm^2. This design demonstrates other benefits in low power consumption and area compared with other ring oscillators.

KEYWORDS

differential ring VCO, low power, wide tuning range

1 | INTRODUCTION

Recently, high-speed wireless and communication systems that have wide tuning range have attracted a lot of attention. In modern wireless and communication systems, phase-locked loop (PLL) plays a critical role.[1] PLL systems are composed of phase detector (PD), loop filter (LF), charge pump (CP), and voltage-controlled oscillator (VCO). The VCO is the most vital part of the PLL because it directly provides the output signal of the PLL. The PLL is a closed-loop feedback system that estimates the frequency and phase angle of its input signals when it is in lock. On the other hand, oscillator is an amplifier with the positive feedback loop in which the frequency is the function of the voltage.[2-7]

VCOs can be classified in two types: the LC-VCO and ring-VCO.[1] Each type has different frequency tuning methods. For example, variable output capacitor, current steering, and latch control are used for frequency variation of ring oscillator while variable capacitor or variable inductor are used for frequency variation of LC-VCO. LC-VCOs are the best option for radio applications (RFs), and they have the highest resolution and frequency, but they suffer from the limited tuning range and the large chip area. On the other hand, ring-VCOs have many advantages such as wide tuning range, low area, easy integration, multiphase clock generation, and providing high frequency at low power. However, ring-VCOs suffer from poor phase noise performance and low resolution.[8-13]

Ring-VCOs are divided into two categories: single-ended and differential-ended categories. In differential-ended ring-VCO (DRO), the number of delay cells can be odd or even, while for single-ended ring-VCO (SERO), the number of delay cells should be odd. According to the Barkhausen criterion, every cell should add 180°/N phase and N is number of delay cell in ring-VCO. DROs are more popular than SEROs because of their advantages such as possibility of using an odd or even number of cells, better immunity to common mode noise, lower swing, and 50% duty cycle at the output. Moreover, it is easy to achieve very high-frequency performance with both in-phase and quadrature outputs in DROs.[14-21]

From the past, DRO designers have been working to improve the important parameters in designing DROs, such as phase noise, power dissipation, voltage operation, occupied area, oscillation frequency, multiphase clock generation, supply sensitivity, and tuning range. Therefore, different DROs topologies have been proposed to improve these parameters. Park-kim delay cell-based DRO in Tiao and Sheu[22] provide wide frequency range and full range control voltage; however, it consumes high power dissipation. Voltage and current controlled delay cell-based DRO in Eken and Uyemura[23] generates high frequency outputs and wide tuning range, while it suffers from poor phase noise and high power consumption. The wide tuning range attained at low voltage is the main feature of delay cell with symmetric load-based DRO presented in Parvizi et al[24]; however, this oscillator has the poor performance of the phase noise. Besides of the good phase noise and wide tuning range, the DRO with the latch pair delay cell in Lu et al[25] reveals good tuning linearity of the control voltage, but it results in high power dissipation and low frequency. The DRO with the delay cell of injection locking technique in Lee et al[26] is another DRO that has scalability, wide operation frequency range, and low phase noise, but despite the advantages it has, it consumes high power. The proposed classical fully differential delay cell-based DRO topology in Sanchez-Azqueta et al[27] can significantly save the area and reduce the power consumption but at the expense of narrow frequency range. Shunt-Shunt feedback delay cell-based DRO in Tu et al[28] improves not only the tuning frequency range but also the output signal swing and power consumption. DRO implemented with delay cell with push-pull inverters in Liu et al[29] provides high frequency and introduces problems, such as the limited frequency tuning range, poor phase noise performance, and high power consumption. A delay cell with cross-coupled symmetric load-based DRO with wide frequency range, good linearity, and low power is proposed in Li and Lin.[30] DRO with programmable resistive network-based delay cell in Fahs et al[31] has wide frequency range, but its power consumption is high. The wide tuning range DRO implemented with delay cell in Yoo et al[32] offers the good phase noise performance; however, the high power consumption and large chip area have become critical drawbacks in this DRO. The DRO in Demartinos et al[33] exhibits wide frequency range, but on the other hand, it consumes more power.

In this paper, a four-stage DRO is proposed. In this VCO, several techniques have been used to increase the frequency range. It has wide tuning range, high frequency, low power, and low occupied area.

This brief is organized as follows: Section 2 describes the proposed VCO. The simulation results are given in Section 4. Finally, Section 5 concludes the paper.

2 | PROPOSED DRO-BASED VCO

In DROs, the number of stages can be odd or even. But increasing the number of stages leads to increased power consumption, area, and cost. Therefore, two-, three-, or four-stage DROs are more common. Two- and four-stage DROs have the capability of generating a quadrature output, but if oscillation frequency is important, three-stage DROs is more appropriate than four-stage DROs. The use of two-stage DRO seems to reduce power consumption, but when designing a two-stage DRO, in order to satisfy the Barkhausen criteria, an additional phase shift for each cell is required. On the other hand, additional power is consumed to achieve the appropriate phase shifts.[34]

The proposed four-stage DRO is shown in Figure 1. In this DRO, dual-delay loop scheme for high operation frequency is applied.[35-37] The dual-delay loop is composed of the primary delay path with higher delay and the secondary delay path with lower delay. In Figure 1, the dotted line indicates the secondary delay path and the solid line indicates the primary delay path. Each of four delay cells in this DRO has two differential primary input voltages of the Vin1+ and Vin1−, two differential secondary input voltages of the Vin2+ and Vin2− that come 45^0 earlier in phase than Vin1+ and Vin1−, and two differentially output voltages of the Vout1+ and Vout1−. In delay cells of the proposed DRO, Vin1+ and Vin1− are given from the Vout1+ and Vout1− of the previous delay cells, and Vin2+ and Vin2− are connected to the Vout1+ and Vout1− of the two previous delay cells.

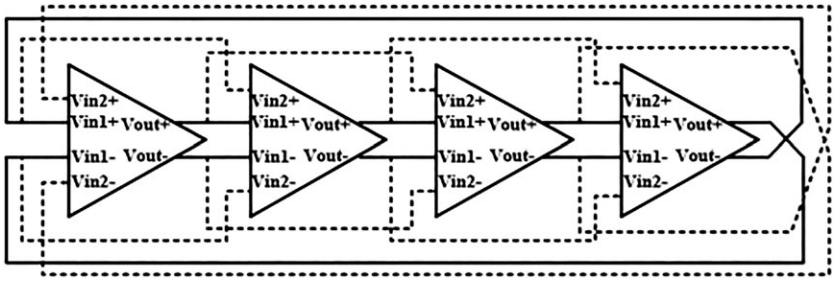

FIGURE 1 The proposed four-stage DRO-based voltage-controlled oscillator (VCO) with solid line for primary delay path and dotted line for secondary delay path[35]

The structure of the delay cell of VCO presented in Kim et al[38] is shown in Figure 2. M1 and M2 in the differential delay cell shown in Figure 2 are differential input NMOS transistors and their gate is connected to the primary input. M3 and M4 are the cross-coupled PMOS transistors, M5 and M6 are the PMOS input transistors that connected to the secondary delay path and Mcont1 and Mcont2 are the PMOS control transistors that their task is to change the frequency of the DRO oscillation by changing the control voltage. Each cell has two differential outputs, and this DRO has a total of eight output phases.

By inspiring the technique available at Kim et al,[38] the delay cell shown in Figure 3 with two control voltages is proposed. In this delay cell, M1 and M2 are differential input NMOS transistors of the primary loop, M5 and M6 are cross-coupled load PMOS transistors for providing a positive feedback latch and to increase the swing they are connected to the V_{dd}, and M3 and M4 are the differential input PMOSs. The performance of the PMOS is usually slower than the NMOS. Therefore in the proposed delay cell for compensating the performance of the M3 and M4 PMOSs, the input of these two PMOSs is connected to the secondary input. In this delay cell, to achieve a wide frequency range, two control voltages are applied. M7, M8, and M9 are the control transistors, and the input of the M7 and M8 PMOS transistors are connected to the control voltage of the Vctr2 and the input of the M9 NMOS transistor is connected to the control voltage of the Vctr1. M7 and M8 control PMOS transistors are used to obtain high frequencies. On the other hand, the NMOS control transistor of the M9 is low-threshold voltage NMOS and is applied to obtain low frequencies. In addition, the Vctr1 should be greater than V_T of the M9 to keep the M9 transistor ON and as V_T becomes smaller, Vctr1 can also be set to smaller values. Therefore in the proposed delay cell for increasing the variations range of the Vctr1 and frequency of the proposed VCO, M9, the low-V_T NMOS transistor, is used in the proposed delay cell.

When Vctr2 is set to high value, the driving current of M9 can be increased by increasing the voltage value of the Vctr1. Therefore, the discharge speed of the load capacitor of the proposed delay cells is increased. As a result, the delay of the delay cell is reduced and so the proposed VCO frequency is increased. In the case of the Vctr1 is set to high value, by decreasing Vctr2, M7 and M8 become more ON and the effect of the transistor M3 and M4 that are connected to the

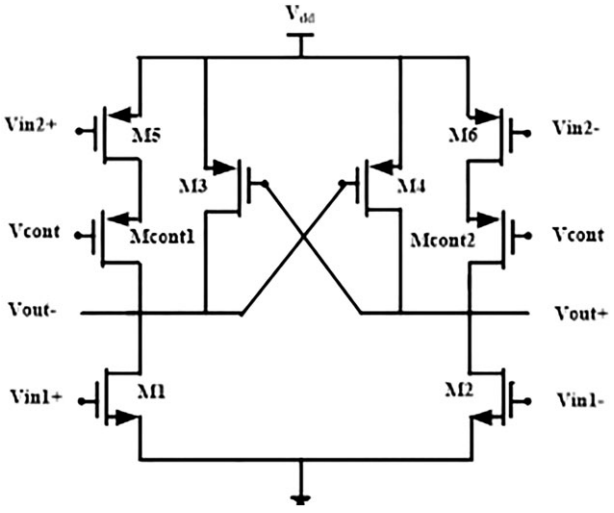

FIGURE 2 The delay cell of the voltage-controlled oscillator (VCO) presented in Kim et al[38]

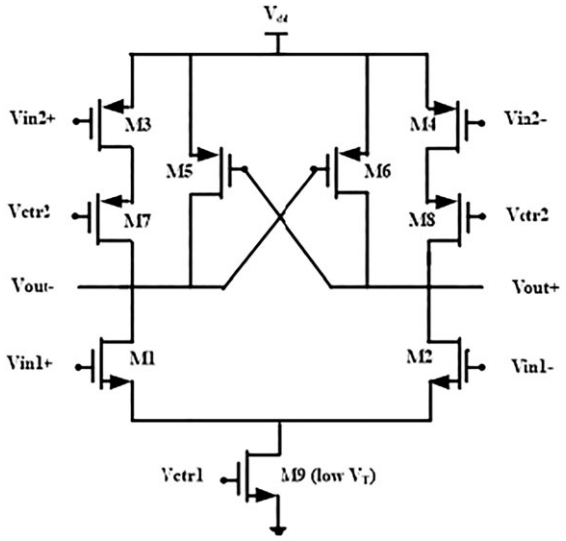

FIGURE 3 Proposed delay cell

secondary input starts to be increased. As a result of increasing the effect of the M3 and M4, the effect of the second path on the delay cell begins to increase. Therefore, the driving current of the pull down network of the proposed delay cells is increased. Consequently, the load capacitor of the proposed delay cell can be charged at a faster rate. This increasing in speed of the charging the load capacitor culminates in reducing the delay of the delay cell and subsequently increasing the frequency of the proposed VCO.

The sizing of the transistors used in the proposed VCO cells is presented in Table 1.

3 | FREQUENCY ANALYSIS

In Hafez and Yang[39] and Sun and Kwasniewski,[40] a general model for multipath ring oscillators having arbitrary coupling structures is presented to calculate the oscillation frequency. In addition, Hafez and Yang[39] and Sun and Kwasniewski[40] determine the oscillation frequency as a function of number of stages and delay loops. On the other hand, in the proposed paper, an analysis is presented to examine the factors affecting the speed of the output voltage changes of the proposed delay cell.

The proposed VCO works in two different modes: low frequency and high frequency. In the low-frequency mode, the output waveform is square. To achieve low frequencies in the proposed VCO, the effect of M3 and M4 transistors should be eliminated, because the secondary inputs of the proposed delay cell that increase the VCO's speed are applied to these transistors. For this purpose, the input of Vctr2 is set to high value. In this case, the equivalent half-circuit is shown in Figure 4A.

In a low-to-high transition of Vin1+, the delay cell exhibits three regions of operation. In the first region, $|V_{GS5}|$ is V_{dd} and therefore M5 is ON. Since the input of the M1 has low value, V_{GS1} is lower than V_{Tn} (the threshold voltage of NMOS transistors), so this transistor is off. In this region $I = -I_{D5}$ and therefore I is independent of the variation of Vctr1 according to Equation 1.

$$I_{D5} = \mu_p C_{ox} \frac{W_9}{l_9} \left(\left((V_{out+}) - V_{dd} - V_{Tp} \right) \left((V_{out-}) - V_{dd} \right) - \frac{1}{2} \left((V_{out-}) - V_{dd} \right)^2 \right). \quad (1)$$

TABLE 1 The sizing of the transistors used in the proposed VCO cells (l = 65 nm)

Transistor Name	M1, M2, M3, M4, M7, M8	M5, M6	M9
Transistor width, μm	1.56	0.91	3.12

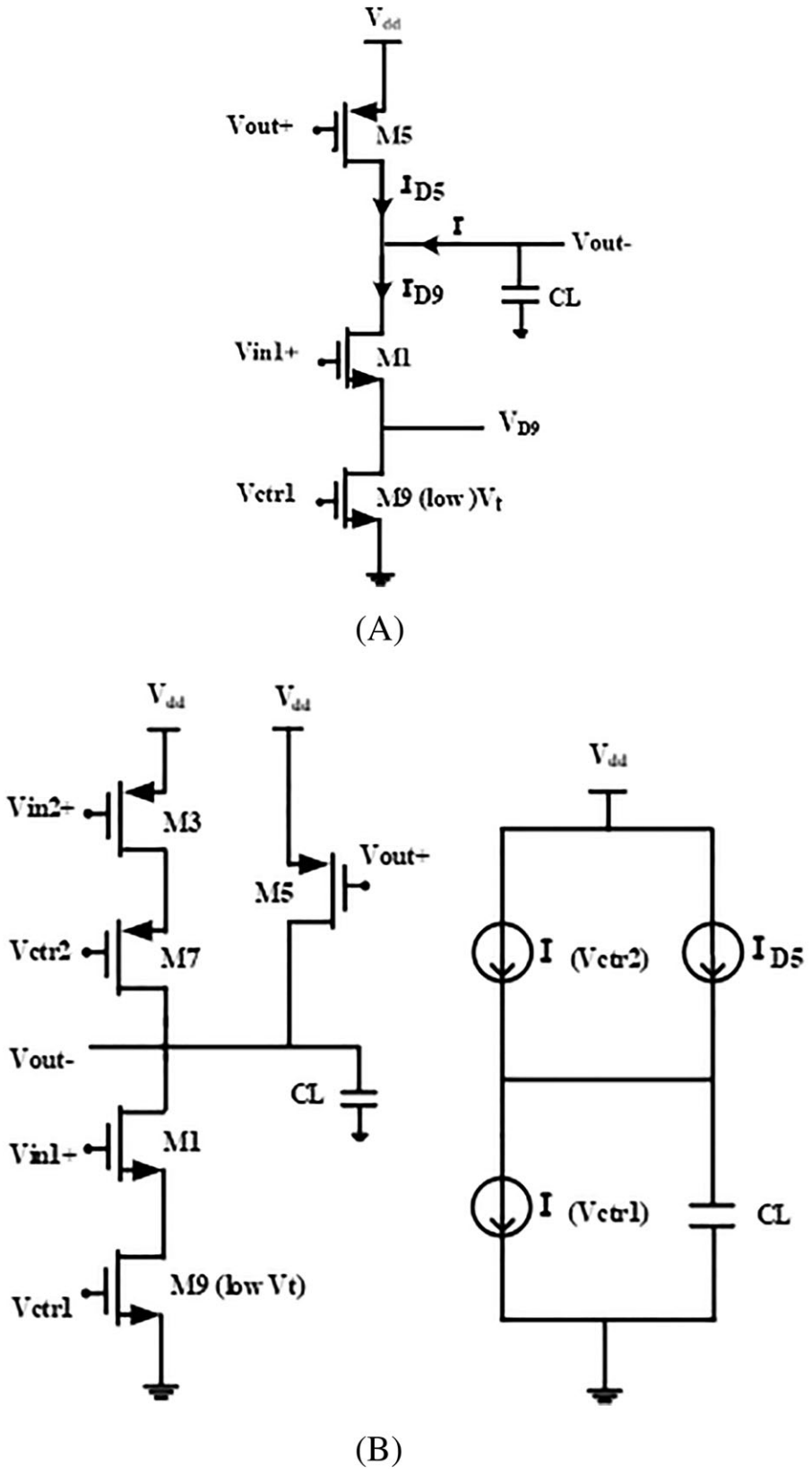

FIGURE 4 Half-circuit of the proposed delay cell in (A) low-frequency mode (B) high-frequency mode

In the second region, $|V_{GS5}|$ is higher than $|V_{Tp}|$ (the threshold voltage of PMOS transistors) and this transistor is ON; on the other hand, V_{GS1} is higher than V_{Tn} and M1 is ON. So in the second region, $I = I_{D9}(\text{Vctr1}) - I_{D5}$, and according to Equations 1 and 2, I_{D5} is independent of the variation of Vctr1 but I_{D9} depends on it.

$$I_{D9}(vctr1) = \mu_n C_{ox} \frac{W_9}{l_9} \left((Vctr1 - V_{Tn\ low})\ V_{D9} - {}^{1}/_{2} V_{D9}{}^{2} \right). \tag{2}$$

Therefore, I depends on Vctr1 and as Vctr1 increases, I is increased. On the other hand, cell delay can be reduced if Vctr1 is increased according to Equations 2, 3, and 4.

$$I\,\Delta t = C_L \Delta V_{out-} = C_L \frac{V_{dd}}{2}, \tag{3}$$

$$\Delta t = C_L \frac{V_{dd}}{2I}. \tag{4}$$

In the third region, $|V_{GS5}|$ is lower than $|V_{Tp}|$ and M5 is off while V_{GS1} is higher than V_{Tn} and M1 is ON. So $I = I_{D9}$(Vctr1) and therefore according to Equation 2, in this region as the second region, I depends on Vctr1. But in this region, this dependency is greater. In the third region, according to Equations 2, 3, and 4, the increase of Vctr1 will result in decreasing the delay of the delay cell and increasing the frequency of the proposed VCO.

In all three regions, the VCO output frequency is independent on the Vctr2. In order to achieve the low frequencies, Vctr2 is set to the high value and only by changing Vctr1 the VCO frequency is changed. Also, according to Equation 2, using low-V_T NMOS transistor of the M9 in proposed delay cell causes the increment of Vctr1 variations range.

In the high-frequency case, the equivalent half-circuit of the proposed VCO is illustrated in Figure 4B. In this case, the oscillation frequency of a common ring oscillator can be defined with a large signal model as

$$f_{osc} = \frac{1}{N\left(t_{rise} + t_{fall}\right)}, \tag{5}$$

where N is the number of stages of the ring oscillator, t_{rise} is the rising time of the output signal, and t_{fall} is the falling time of the output signal. For this delay stage, t_{rise} and t_{fall} can be obtained from

$$I_{discharge} = C_L \frac{d\,V_{out}}{dt} \Rightarrow \int_0^{t_{rise}} \frac{I_{D9}(Vctr1) - I_{D5}}{C_L} \mathrm{dt} = \int_{0.1V_{dd}}^{0.9V_{dd}} d\,V_{out} \Rightarrow t_{rise} = 0.8 \frac{C_L V_{dd}}{I_{D9}(Vctr1) - I_{D5}}, \tag{6}$$

$$I_{charge} = C_L \frac{d\,V_{out}}{dt} \Rightarrow \int_0^{t_{fall}} \frac{I_{D7}(Vctr2) + I_{D5}}{C_L} \mathrm{dt} = -\int_{0.9V_{dd}}^{0.1V_{dd}} d\,V_{out} \Rightarrow t_{fall} = 0.8 \frac{C_L V_{dd}}{I_{D7}(Vctr2) + I_{D5}}. \tag{7}$$

As a result, the contribution of rising and falling transitions are included in Equation 8:

$$f_{osc} = \frac{1}{1.6NC_L V_{dd} \left(\frac{1}{I_{D9}(Vctr1) - I_{D5}} + \frac{1}{I_{D7}(Vctr2) + I_{D5}} \right)} = \frac{(I_{D9}(Vctr1) - I_{D5})(I_{D7}(Vctr2) + I_{D5})}{1.6NC_L V_{dd}(I_{D9}(Vctr1) + I_{D7}(Vctr2))}. \tag{8}$$

To achieve high frequency of the proposed VCO, Vctr1 is set to high value so that the resistance of the M9 is kept to a minimum. As the resistance of the M9 decreases, the resistance of the discharge path of the load capacitor (C_L) will also decrease and the discharge stream of the C_L is reduced accordingly. As a result, according to Equation 4, the delay of the proposed delay cell is decreased and the VCO frequency is increased. Equation 8 and Figure 4 show that the output frequency depends on the control voltages. On the other hand, in higher frequency due to the fact that Vctr1 is kept constant to high value, the output frequency is changed only by changing the Vctr2.

In Equation 8, the oscillation frequency seems to be inversely proportional to V_{dd}, but it is not correct. Oscillation frequency is proportional to I_{D5} according to Equation 8. On the other hand, I_{D5} has a quadratic relationship with V_{dd} according to Equation 1. Therefore, oscillation frequency is proportional to V_{dd} according to Equation 8.

The gate of the input PMOS M3 is connected to the secondary input of Vin2+. Therefore, the PMOS M3 receives its input earlier than input NMOS M1 connected to the primary input, which can compensates the PMOS speed limitation. As a result, the delay of the proposed delay cell is decreased and the VCO frequency is increased. On the other hand, by reducing Vctr2, the M7 transistor is turned ON. In this case, the effect of the transistor M3 is increased. Since the

secondary input increases the VCO's speed, by increasing the effect of the M3 transistor, the VCO output frequency is increased. Conversely, by decreasing Vctr2 and subsequently reducing the effect of secondary input on the delay cell, the frequency of the VCO is decreased.

4 | SIMULATION RESULTS

The proposed DRO-based VCO is simulated in 65-nm TSMC CMOS technology in Cadence software under 1.2-V supply voltage. The three-dimensional graph of frequency variation in terms of Vctr1 and Vctr2 changes are shown in Figure 5. By varying the Vctr1 from 0.23 V to 1.2 V when the Vctr2 is fixed at 1.2 V, the frequency of the proposed VCO is changed from 1 MHz to 5.161 GHz, while VCO frequency changing is between 5.161 up to 13.8 GHz by varying the Vctr2 from 1.2 V to 0 V when the Vctr1 is fixed at 1.2 V. So the VCO can oscillate from 1 MHz to 13.8 GHz with a frequency range of 13.799 GHz (99.99%). On the other hand, as can be deduced from Figure 5, frequency variations based on Vctr2 are small in low frequencies. In this case, Vctr1 and Vctr2 can be used for coarse and fine frequency changes, respectively. At high frequencies, the role of these two control voltages are replaced with each other and frequency changes based on Vctr1 is less, while by changing Vctr2 more changes can be observed. In the other words, in high frequencies, Vctr1 can be used for fine variations and Vctr2 for coarse variations. In the middle frequencies, according to the values of Vctr1 and Vctr2, each of them may have coarse or fine role.

The phase noise of the proposed VCO as seen in Figure 6 reaches to −82.3 dBc/Hz at 1 MHz offset frequency and −106.9 dBc/Hz at 10 MHz offset frequency from 5.161 GHz center frequency (Vctr1 = 1.2, Vctr2 = 1.2).

The power consumption of the proposed VCO is changed between 1.715 mW down to 29.3 μW.

For better comparison with other VCOs at different center frequencies, usually, figure-of-merit (FOM) that is calculated from Equation 9 is used[34]:

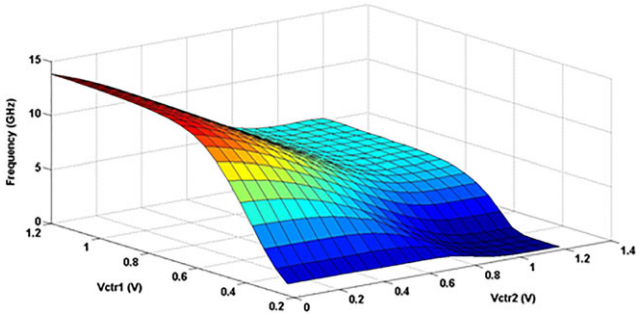

FIGURE 5 The frequency variation curve in terms of Vctr1 and Vctr2 changes [Colour figure can be viewed at wileyonlinelibrary.com]

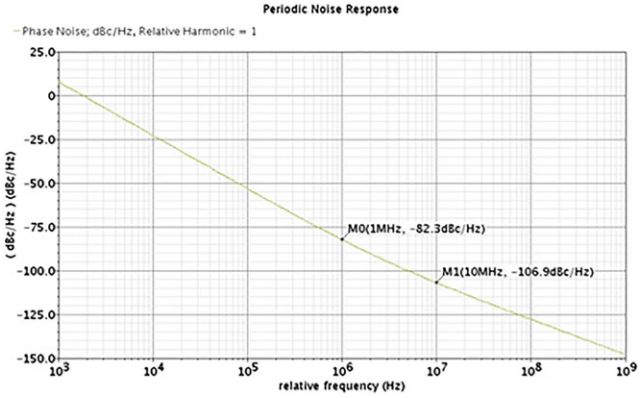

FIGURE 6 Simulated phase noise performance of the proposed voltage-controlled oscillator (VCO) [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 2 Variation in VCO parameters as a function of process, temperature and voltage

	Temperature Variations (V_{dd} = 1.2 V)			**Voltage Variations (T = 27°C)**				**Process Variations (V_{dd} = 1.2 V)**		
Parameters	**T = −25°C**	**T = 0°C**	**T = 75°C**	**V = 1 V**	**V = 1.1 V**	**V = 1.2 V**	**V = 1.3 V**	**Slow-worst (process = slow NMOS and PMOS; T = 75°C)**	**Typical (T = 27°C)**	**Fast-best (process = fast NMOS and PMOS; T = −25°C)**
Tuning range, GHz	0.276×10^{-3} − 14.58	0.505×10^{-3} − 14.16	8.12×10^{-3} − 13.08	0.965×10^{-3} − 10.75	0.984×10^{-3} − 12.28	1×10^{-3} − 13.8	1.019×10^{-3} − 15.08	0.994×10^{-3} − 11.14	1×10^{-3} - 13.8	1.02×10^{-3} - 16.89
f_{osc}, GHz (Vctr1 = 1.2 V, Vctr2 = 1.2 V)	5.478	5.321	4.945	3.93	4.563	5.161	5.725	4.109	5.161	6.634
P_{diss}, mW	0.802	0.799	0.770	0.413	0.582	0.785	1.024	0.634	0.785	0.964

$$FOM = L\left\{f_{Off}\right\} - 20\ \log\frac{f_{OSC}}{f_{Off}} + 10\ \log\frac{P}{1mW}, \tag{9}$$

where L{f_{Off}} is the phase noise of the oscillator in dBc/Hz at the offset frequency (f_{Off}), f_{osc} is the center frequency and P_{diss} is the power dissipation in milliwatts. But this FOM equation is not very comprehensive. Therefore, in this paper, for improving the FOM to be able to better compare the VCO parameters, two other terms including frequency range and occupied area have been added to Equation 9. FOM is developed as Equation 10:

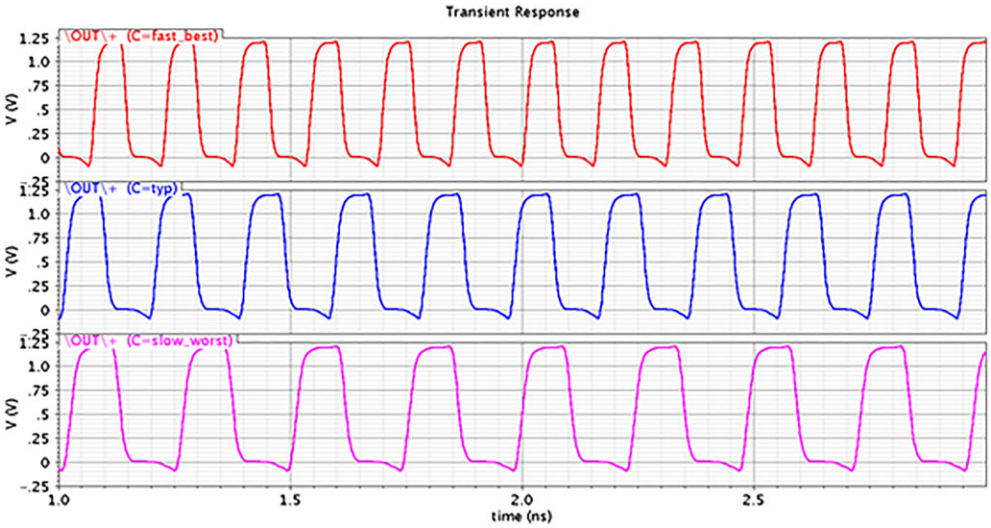

FIGURE 7 The waveform of the center frequency of the proposed voltage-controlled oscillator (VCO) for the fast-best, slow-worst, and typical mode [Colour figure can be viewed at wileyonlinelibrary.com]

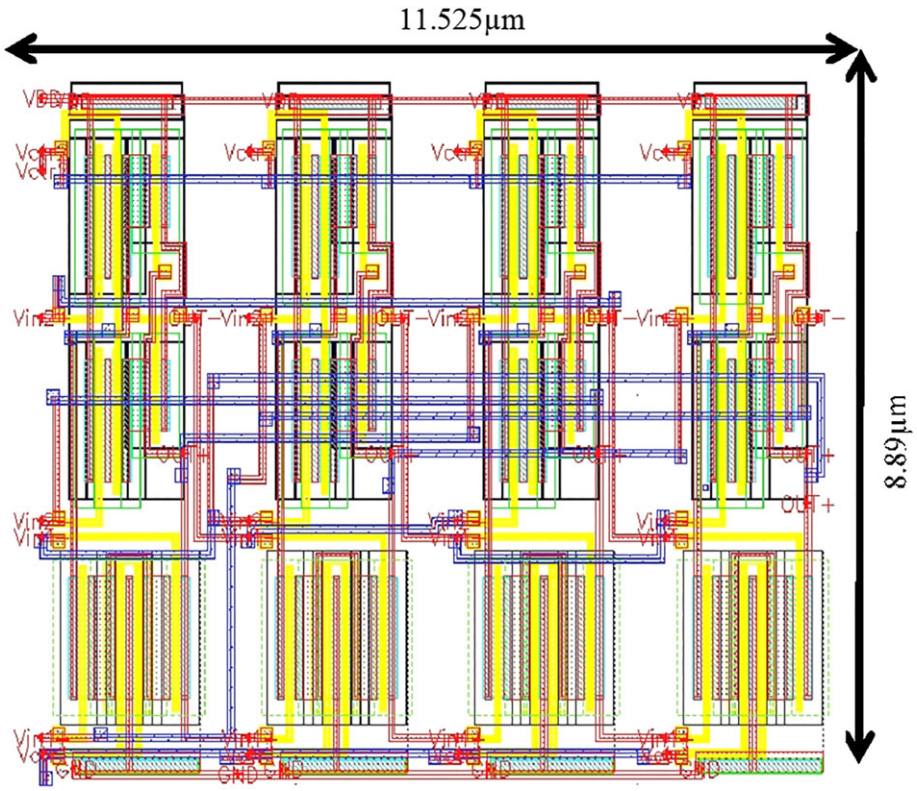

FIGURE 8 Layout of proposed four-stage voltage-controlled oscillator (VCO) [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 3 Performance comparison

Reference	Technology, nm	Supply, V	Number Stage	Tuning Range, GHz	Active area, μm^2	f_{osc}, GHz	Phase Noise, dBc/Hz at 1 MHz	P_{diss}, mW	FOM, dBc/Hz	Results
Kamran and Ghaderi[36]	180	1.8	3	3.1-10.1 (69.3%)	-	6.6	−113	6.01 at maximum frequency	-	Simulation
Chien et al[13]	20	1.25/1.1	4	2-16 (87.5%)	44×10^3	15	−136.6 at 10 MHz	46.2	−212.395	Measurement
Sharma and Biswas[20]	65	0.7	3	0.83-3.77 (77.98%)	67.65	-	-	26.73×10^{-3}	-	Measurement
Yoo et al[32]	65	1.2	2	2-8 (75%)	38×10^3	4.2	−101	6.4	−193.744	Measurement
Sun and Jiang[37]	180	1.2	3	0.261-1.32 (80.22%)	5.175×10^3	0.73	−98	0.41-1.6	−189.796	Simulation
Kim et al[38]	65	1	4	0.48-1.01 (52.47%)	22.54×10^3	0.645	−110.8	10	−182.689	Measurement
Mishra and Sharma[1]	180	1.8	3	1.0229-3.995 (74.39%)	-	3.995	−80.17	7.49	-	Simulation
Vornicu et al[21]	180	1.8	4	0.4-0.85 (52.94%)	812	0.85	−102 at 2 MHz	1.17	−182.38	Measurement
Demartinos et al[33]	65	1.2	4	1.55-3.9 (60.25%)	-	3	−94	7.68	-	Measurement
This work	65	1.2	4	0.001-13.8 (99.99%)	102.457	5.161	−82.3	0.785	−193.573	Simulation

$$FOM = L\left\{f_{Off}\right\} - 20\log\frac{f_{OSC}}{f_{Off}} - 20\log\left(100\,\frac{F_{MAX} - F_{MIN}}{F_{MAX}}\right) + 10\,\log\frac{P}{1mW} + 2\,\log\frac{area}{1\mu m^2}, \tag{10}$$

where F_{MAX} is the maximum frequency, F_{MIN} is the minimum frequency, and area is the occupied area in square micrometers. The calculated FOM of the proposed VCO is −193.573 dBc/Hz.

The process, voltage, and temperature (PVT) variation analysis is done for the proposed VCO for the purpose of evaluating PVT sensitivity. The simulation of the PVT variation results are listed in Table 2. In this analysis, the tuning range, center frequency, and power dissipation are simulated. As seen in Table 2, by increasing the temperature, the tuning range, f_{osc}, and power dissipation of the proposed VCO is decreased. On the other hand, these three parameters are increased by increasing the supply voltage. In addition, the tuning range, f_{osc}, and power dissipation of the proposed VCO in fast-best mode are more than typical mode and in typical mode are more than slow-worst mode. These PVT variation results are acceptable.

The waveform of the center frequency of the proposed VCO for the fast-best at −25°C, slow-worst at 75°C, and typical mode at 27°C and under 1.2 V supply voltage is shown in Figure 7.

The layout of the proposed four-stage VCO shown in Figure 8 is estimated about 102.457 μm^2.

In Table 3, the performance of the proposed VCO pre-layout simulation is compared with that of other recent VCOs in 65 nm technology. Using of transistors with a large $^{W}/_{L}$ ratio in VCO improves phase noise but increases the active area and power consumption. In proposed VCO, small transistors are used to reduce the power consumption and active area. As seen in this table, the proposed VCO has a very low power consumption and area. The tuning range of this work has been improved by 19.77% compared with other works in table. It also presented acceptable phase noise. In the last column of this table, the FOM of the VCOs is calculated using the improved FOM in this paper. In this table, proposed VCO and presented VCOs in previous works[1,36,37] have simulation results, while other VCO in table presented measurement results.

5 | CONCLUSION

In this paper, a novel multipath delay cell for four-stage VCO with wide frequency tuning range was proposed. It has two control voltages for changing the frequency. Low-V_T NMOS transistor is used in this delay cell to achieve a wide tuning range. In addition, in this paper, the analytical study of the factors affecting the speed of the output voltage changes of the proposed delay cell is presented. The proposed VCO is simulated in 65-nm TSMC CMOS technology in Cadence software under 1.2-V supply voltage. This VCO has wide tuning range of 1 MHz to 13.8 GHz (99.99%), acceptable phase noise of −82.3 dBc/Hz at 1 MHz offset frequency, and −106.9 dBc/Hz at 10 MHz offset frequency from 5.161 GHz center frequency, the achieved low power of 0.785 mW and low occupied area of 102.457 μm^2. Therefore, this oscillator is suited for the applications with high frequency, wide frequency range, low power, and low area.

ACKNOWLEDGMENT

We would like to thank Dr. Fiorelli, Rafaella (RF/analog IC Designer at IMSE-CNM, Sevilla, Spain) for her feedback and contribution.

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How to cite this article: Askari S, Saneei M. Design and analysis of differential ring voltage controlled oscillator for wide tuning range and low power applications. *Int J Circ Theor Appl*. 2019;47:204–216. https://doi.org/10.1002/cta.2582