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A CMOS based low power digitally controlled oscillator design with MOS varactor

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Abstract
With the shift from traditional analog circuit designs to an all-digital intensive approach, the all-digital Phase-locked loops (ADPLLs) have become more attractive in digital communication systems. Digitally controlled oscillators (DCO) are the key components of the ADPLL circuits. In this paper, a new low power DCO structure is proposed with NMOS transistor as the switching network and utilizing the NMOS varactor as shunt-capacitive loads for the delay cells. The new DCO is capable of producing much higher output frequencies and comprises of components that are fully digital. The proposed DCO structure is designed for three, five and seven stages in CMOS 0.18 μm technology. Variable capacitance is achieved by the use of control word which is applied through NMOS switches conditionally selecting combinations of capacitance and hence determining the delay of the circuit. A 3-stages digitally controlled oscillator shows output frequency variation from 1.986 to 3.526 GHz with a power consumption of 1.484 mW. In the 5-stages DCO, the output frequency varies from 1.154 to 2.210 GHz with a power consumption of 2.762 mW. For 7-stages DCO, the output oscillation frequency is in the range from 0.835 to 1.658 GHz with a power consumption of 4.04 mW. A 3-stages DCO shows a phase noise of − 100.06 dBc/Hz with the offset of 1 MHz with the corresponding figure of merit (FoM) of 165.37 dBc/Hz. Five and seven-stages DCO show phase noise of − 102.08 dBc/Hz and − 105.52 dBc/Hz at 1 MHz respectively. The figure of merit (FoM) for 5 and 7-stages is 160.92 dBc/Hz and 159.07 dBc/Hz respectively. The digital tuning range for 3, 5, and 7-stages DCO is 55.96%, 62.78%, and 66.05% respectively. Further, the results show that the designed DCO has a maximum supply voltage tuning range of 101.45% with the variation of V_{DD} from 1 to 1.8 V. Comparison with earlier reported circuits has been made based on output frequency, power consumption, and phase noise.

Keywords ADPLL · Delay cell · Digitally controlled oscillators (DCO) · NMOS · Power consumption · Varactor

1 Introduction

Phase-Locked Loops (PLLs) are the fundamental circuit elements of the data transmission system for clock generation and frequency synthesis [1–4]. Conventional PLLs make use of voltage-controlled oscillator (VCO) for varying the oscillation frequency. However, at low-voltage operation, the frequency tuning for analog CMOS oscillator becomes more difficult to achieve. Also, conventional CMOS based oscillator shows more power consumption and are less immune to the noise. To overcome these issues, all-digital phase-locked loops (ADPLL) have come into existence [5–9]. ADPLL consists of three main components: a digital phase detector, a digital loop filter and a digitally controlled oscillator (DCO).

DCO which is a fully digital-intensive approach, is the key component in the fully digital PLLs for controlling the frequency of oscillation. Digital circuits are more preferable than analog circuits due to the decreasing cost of implementation in the present-day CMOS process technology. Digitally controlled delay elements (delay cells/DCDE) are the main components of DCO. The output frequency of a ring type oscillator is dictated by the delay

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(t_d) offered by single stage as well the number of delay stages (N) and is given by Eq. (1).

$$f_o = 1/2Nt_d \quad (1)$$

In the literature different types of DCO circuits have been reported with one or more approaches [8–15]. The most popular approach as shown in Fig. 1(a), is based on the ring-based inverter topology in which MOS capacitors are used as the switching networks which are binary weighted and are used to modify the delay of the circuit [10, 11]. However, an increase in the number of switched capacitors puts a limitation on the maximum achievable frequency by the DCO. Further, the second approach includes path selection as shown in Fig. 1(b), in which the output frequency can be controlled by selecting the number of delay stages. In path selection, multiplexers are used to select the number of delay stages in the DCO. Path selection is often used in combination with other techniques due to its limited resolution which further increases the hardware requirement [8, 12–15]. The third approach is based on current-starved inverter as given in Fig. 1(c). Binary-weighted NMOS/PMOS switching networks are connected in series with the inverters and the resistance posed by the switching networks is used to modify the delay offered by each stage which in turn dictates the output frequency of the DCO. The current starved inverter based DCO requires complex hardware and hence consumes more area [8, 9]. Delay cells are the major performance governing block of DCO and delay of these cells can be varied with different techniques like modifying the MOS driving strength: by fixed loading, shunt loading, and resistance variation [10, 16–23]. Although the above-mentioned techniques offer reasonable frequency range but by increasing the number of capacitive elements the maximum achievable frequency is limited. In the proposed DCO architecture the maximum frequency is achieved when all the control bits are 0's, hence eliminating all the parasitic elements from the circuit.

In this paper, a three, five and seven stages DCO architectures with NMOS based varactor and switching network have been proposed. The rest of paper is organized as: Sect. 2 describes the proposed design of DCO. Section 3 describes the simulation results followed by a conclusion in Sect. 4.

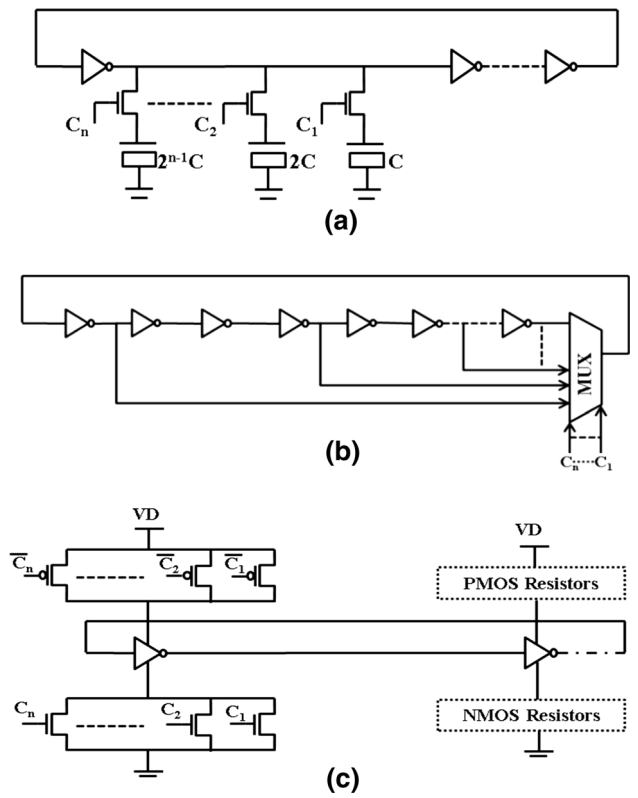

Fig. 1 Conventional DCO techniques: **a** MOS capacitors, **b** path selection, and **c** current starved

2 Proposed DCO circuit design

2.1 Delay element

In the proposed DCO, the delay stage utilizes the MOS varactors as capacitive load cells which produce the delay. For this NMOS transistor is used to realize the MOS varactor by connecting the drain, source, and bulk (D, S, B) of the transistor together as shown in Fig. 2. Since the varactors are implemented using NMOS transistors hence no additional mask is required. Furthermore, transistor based varactors are preferred over diode based varactor since they reduce the static power consumption, area and increases the VCO phase noise performance [24]. The gate acts as one terminal and the drain, source, and bulk connected together to form another terminal of the capacitor with an oxide layer as a dielectric. The gate is connected to the voltage a and the drain, source, and bulk to the voltage b.

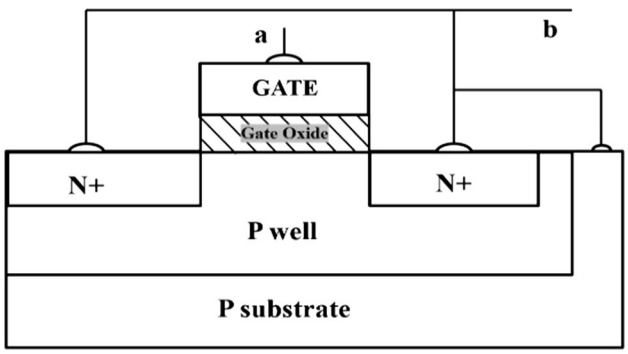

Fig. 2 MOS transistor as MOS varactor

By applying gate voltage greater then threshold voltage i.e. $V_G > V_T$ for NMOS capacitor, an inversion channel builds up due to the surplus electrons on the surface and the MOS capacitor works in strong inversion region. In strong inversion region, the variable MOS capacitance C_{VAR} (maximum MOS capacitance) is dominated by the oxide capacitance C_{OX} given by Eq. (2).

$$C_{ox} = \varepsilon_0 WL/t_{ox} \tag{2}$$

The MOS capacitor can be varied by varying the width of the MOS.

2.2 Delay stage of the proposed DCO

In the conventional DCO, the output frequency is dictated by the delay offered by each delay cell. In the proposed design, a new delay cell with binary weighted and digitally controlled MOS varactor as capacitive loads has been developed. These binary weighted MOS capacitors are used to vary the delay of the stages accordingly thus achieving a large frequency range. Each delay stage has two identical CMOS inverters with capacitive load cells connected between their outputs as shown in Fig. 3. Each capacitive load cell is made of two identical varactors connected in series in between the output lines of the two inverters.

For a 3-bit DCO design, three binary-weighted capacitive loads are connected in between the output lines of the inverters. The NMOS switches connect the node in between the two varactors to ground depending upon the digital binary code applied to them. A control word (D0, D1, D2) is applied through NMOS switches conditionally selecting combinations of capacitance and hence determining the delay of the circuit.

In the proposed DCO, the capacitor is placed before the switch. Subsequently, the off capacitance is reduced to a very small value ($< C_j$), where C_j is the drain junction capacitance of the NMOS switch. As the capacitance seen by each inverter is very small ($< 0.5C_j$), the maximum frequency is achieved when the control word is all zeros. When the switch is ON, the common node between the two MOS varactors is connected to the ground. This makes the ON capacitance to be equal to 2C, where C is the MOS varactor capacitance. As a result of the large difference in the ON and OFF capacitance, large tuning range can be achieved.

Table 1 Width of PMOS and NMOS

MOS varactor	
N3, N4	8.0 μm
N5, N6	4.0 μm
N7, N8	2.0 μm
NMOS switching network	
N9	4.0 μm
N10	2.0 μm
N11	1.0 μm
Inverter	
P1, P2	4.0 μm
N1, N2	2.0 μm
3T-NAND gate	
P3	7.5 μm
P4	2.5 μm
N12	1.25 μm

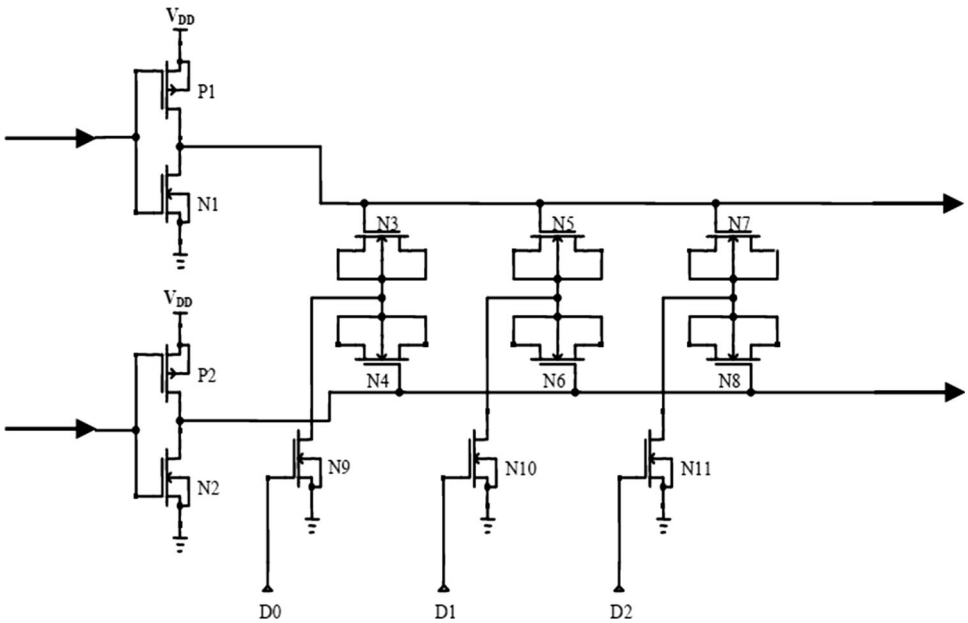

Fig. 3 Proposed delay stage

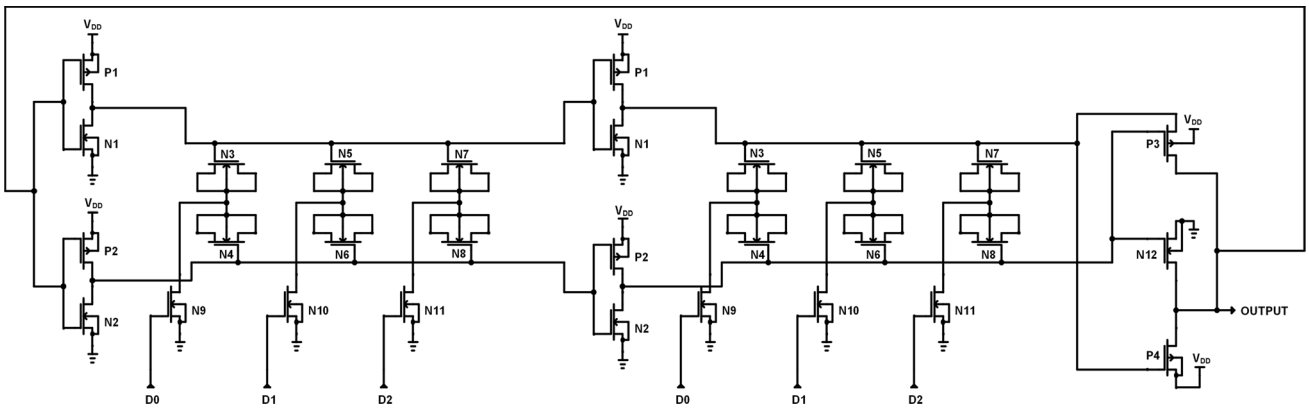

Fig. 4 Proposed 3-stage DCO design

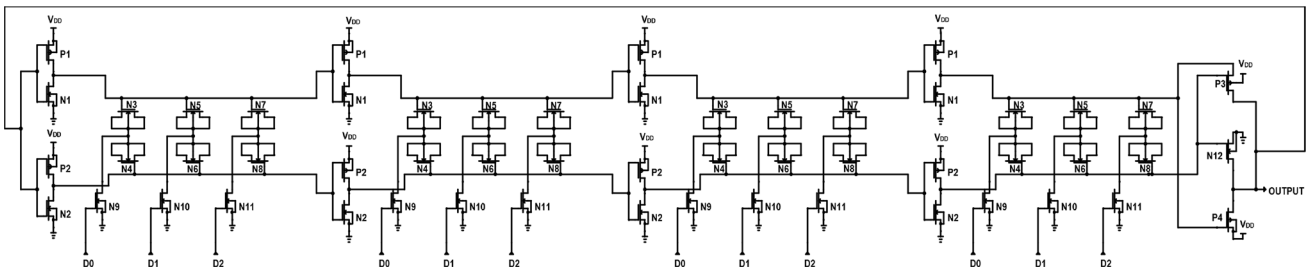

Fig. 5 Proposed 5-stage DCO design

Table 2 Frequency and power consumption variation for 3-bit DCO with NMOS switching network

Control bits			Three-stages DCO		Five-stages DCO		Seven-stages DCO	
D0	D1	D2	Frequency (GHz)	Power consumption (mW)	Frequency (GHz)	Power consumption (mW)	Frequency (GHz)	Power consumption (mW)
0	0	0	3.529	1.484	2.210	2.762	1.658	4.040
0	0	1	3.155		1.950		1.463	
0	1	0	2.871		1.764		1.302	
0	1	1	2.620		1.591		1.170	
1	0	0	2.425		1.455		1.065	
1	0	1	2.245		1.337		0.975	
1	1	0	2.101		1.237		0.897	
1	1	1	1.986		1.154		0.835	

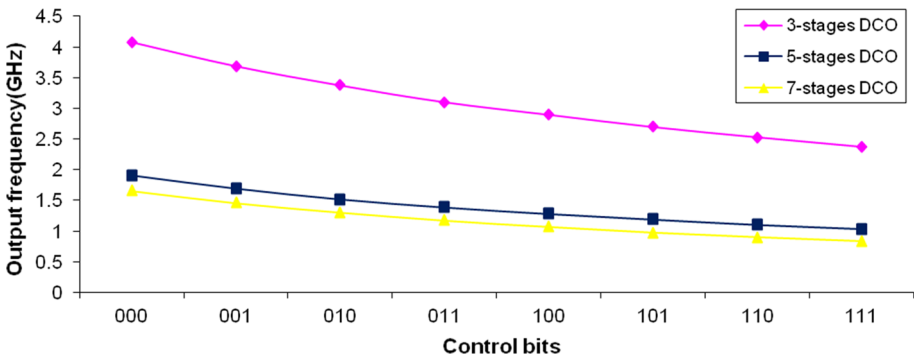

Fig. 6 Output Frequency of 3-bit DCO with three-stages, five-stages and seven stages at V_{DD} = 1.8 V

The width of the PMOS and NMOS transistors of the switching network, MOS varactors, inverters and the 3T-NAND gate is summarized in Table 1.

2.3 DCO circuit design

The new DCO has been designed with 3-stages, 5-stages, 7-stages variant utilizing the proposed delay stage. The proposed DCO design consists of an even number of proposed delay stages and a 3T-NAND gate [25]. The 3-T NAND gate forms the last stage of the DCO making the total delay stages to be odd in number. The 3T-NAND delay stage is made up of two PMOS transistors and one NMOS transistor. The two input terminals of the NAND gate are connected to the two feedback signals from the previous stage. In the 3-T NAND gate, the substrate of PMOS P3 as well as of PMOS P4 is connected to V_{DD} and substrate of NMOS is connected to ground. The delay stages and the 3T-NAND gate form two digital ring oscillators that oscillate at the same frequency and phase.

The NAND gate helps in synchronization of the two oscillators and matches the output of two oscillators in terms of frequency and phase. A 3-bit three-stages DCO has been implemented which consists of two delay stages and a 3-T NAND gate as shown in Fig. 4. The digital control codes have been applied through the NMOS switches which determine the output oscillation frequency.

A 3-bit five-stages DCO has been implemented using the proposed delay stage as shown in Fig. 5. In addition, a 3-bit seven-stages DCO has also been designed using the same methodology and simulations have been carried out in 0.18 μm CMOS technology.

3 Results and discussions

The new DCO has been designed with 3-stages, 5-stages, 7-stages variant utilizing the proposed delay stage in 0.18 μm CMOS technology with 1.8 V supply. To validate the design, the design has been simulated using Mentor graphics tool. Table 2 shows the variation of output frequency and power consumption with respect to control bits applied to a 3-bit DCO for 3-stages, 5-stage and 7-stages DCOs variant. The results show that as the control word is varied from 000 to 111, the output frequency decreases as the delay offered by delay stages increases with increasing MOS capacitance of the varactors of each stage. The results also show that the power consumption does not depend on the control bits but on the number of delay stages as well as on the supply voltage V_{DD}. Figure 6 shows the comparison of the variation of output frequency for 3-stages, 5-stages and 7-stages DCO for a 3-bit control word at supply voltage V_{DD} = 1.8 V.

Table 3 Frequency and Power Consumption Variation for DCO

D0	D1	D2	V_{DD} (V) = 1.0 V		V_{DD} (V) = 1.2 V		V_{DD} (V) = 1.4 V		V_{DD} (V) = 1.6 V		V_{DD} (V) = 1.8 V	
			Frequency (GHz)	Power consumption (mW)	Frequency (GHz)	Power consumption (mW)	Frequency (GHz)	Power consumption (mW)	Frequency (GHz)	Power consumption (mW)	Frequency (GHz)	Power consumption (mW)
0	0	0	1.154		1.828		2.462		3.042		3.529	
0	0	1	1.033		1.645		2.194		2.712		3.155	
0	1	0	0.960		1.492		1.993		2.475		2.871	
0	1	1	0.860	0.008	1.370	0.075	1.820	0.319	2.248	0.790	2.620	1.484
1	0	0	0.805		1.240		1.696		2.094		2.425	
1	0	1	0.729		1.155		1.571		1.939		2.245	
1	1	0	0.682		1.091		1.463		1.814		2.101	
1	1	1	0.644		1.021		1.376		1.687		1.986	

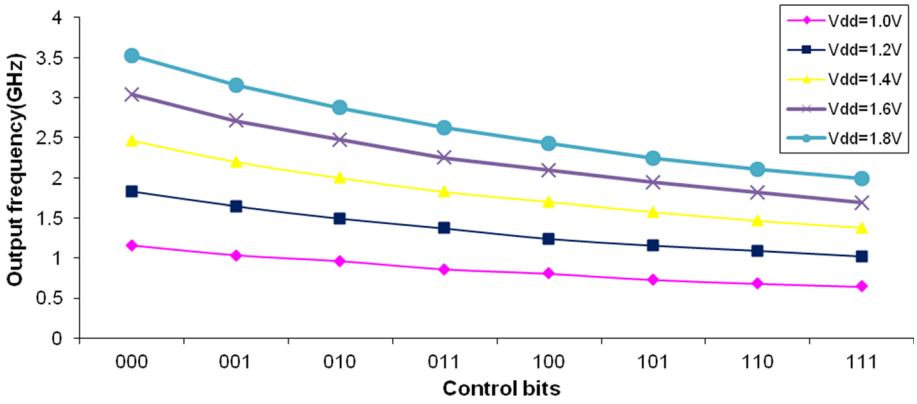

Fig. 7 Variation of output frequency along with varying V_{DD} for a 3-stages DCO

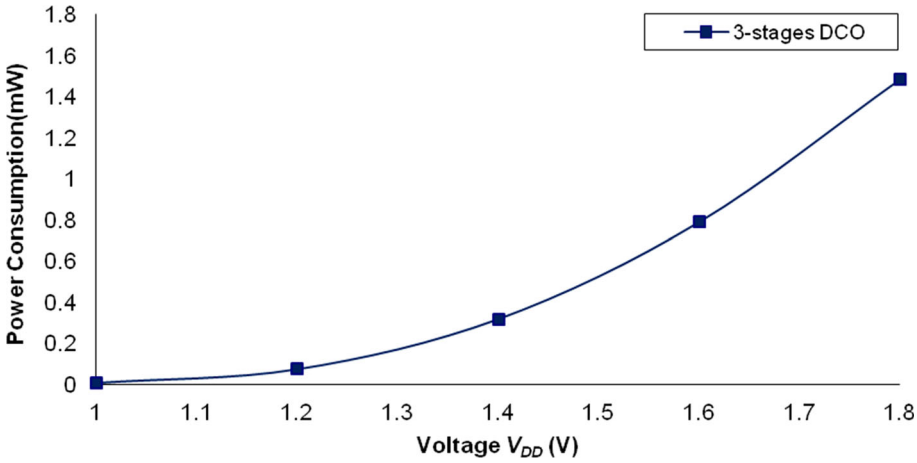

Fig. 8 Power consumption variation with power supply (V_{DD}) variation for proposed 3-stage DCO

Table 3 shows the variation of the output frequency and power consumption with respect to power supply V_{DD} for a 3-stages DCO. Figure 7 shows the variation of the output frequency along with the varying V_{DD} for a 3-stages DCO. The results confirm that the output frequency is sensitive to the changes in the supply voltage V_{DD}.

Supply voltage scaling has proved to be an effective method for reducing the switching power as switching power is quadratically dependent on the supply voltage as given by the following equation:

$$P_{dynamic} = \alpha C_L V_{DD}^2 f_{clk} \tag{3}$$

where α is the activity factor, V_{DD} is the supply voltage, C_L is the total load capacitance and f_{clk} is the clock frequency. The variation of power consumption with varying power supply V_{DD} for a 3-stages DCO is shown in Fig. 8 and the results conform to the quadratic relation between them as given in the above Eq. (3).

The output frequency waveform with control word [000] has been shown for 3-stages DCO in Fig. 9 along with the frequency spectra. Figure 10 shows the output frequency and frequency spectra for 5-stages DCO with control word [101].

The phase noise and figure of merit (FoM) are two essential parameters to measure the quality performance of a ring oscillator. The phase noise of all the three variants of the proposed DCO has been measured as shown in Fig. 11 and the figure of merit (FoM) has been calculated according to the following expression [26]:

$$FoM = 20\log\frac{fc}{f} - 10\log\frac{P_{DC}}{1}mW - L(\Delta f) \tag{4}$$

where $L(\Delta f)$ is the phase noise of the DCO in dBc/Hz at f offset from the carrier frequency f_c, and P_{DC} is the power consumption in mW. Table 4 shows the values of phase noise and FoM for 3,5 and 7-stages DCO along with digital tuning range.

The above results have been compared with the earlier published work as shown in Table 5. It has been observed that the proposed circuit shows a better performance in terms of output frequency and power consumption than the earlier reported circuits. Many DCOs have been implemented with standard inverter-based delay cells, and these circuits suffer from poor performance in terms of power consumption, and output frequency range. In the proposed design of DCO, the output frequency is tuned using the I-MOS based varactor at the output node. The proposed

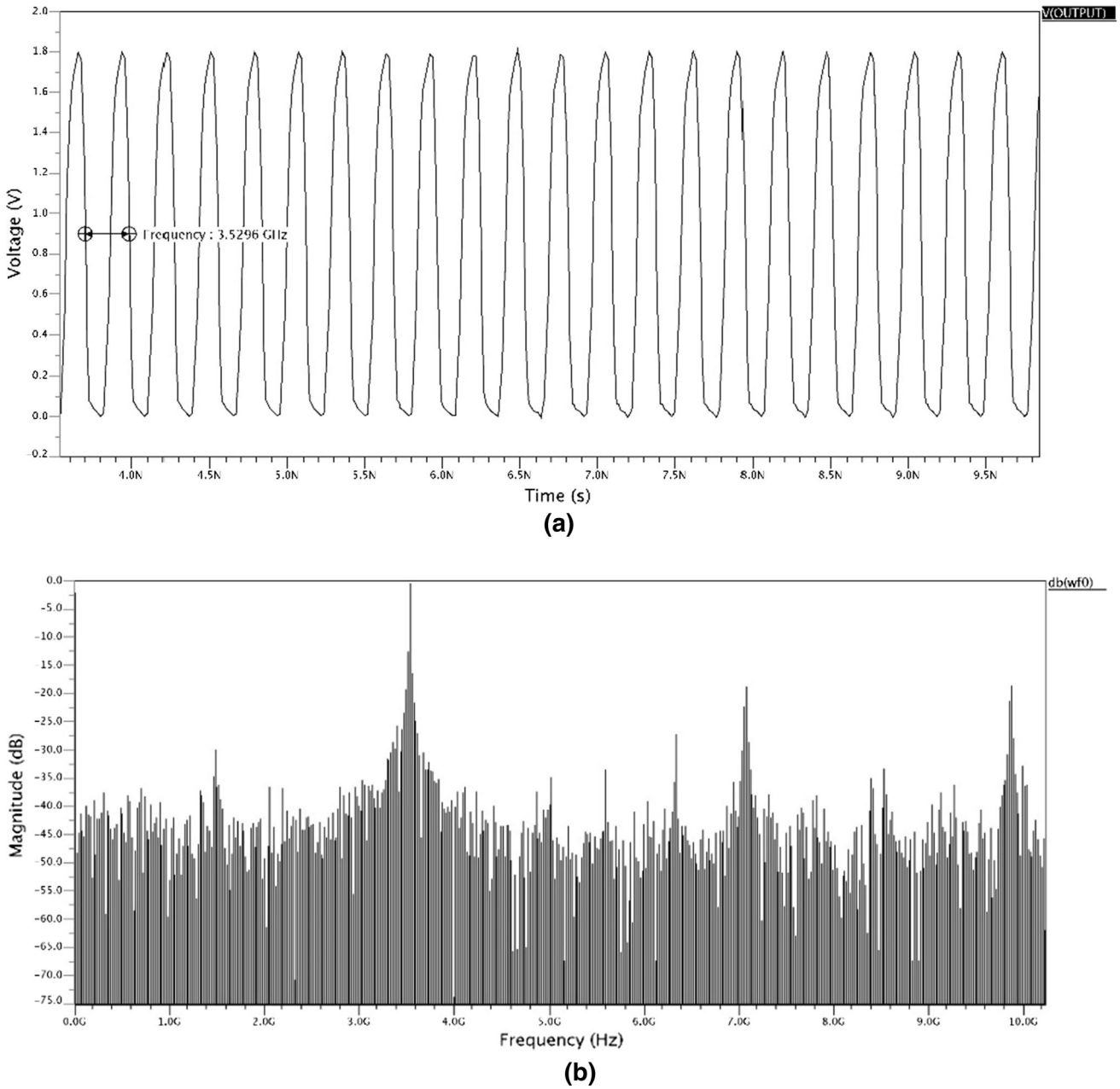

Fig. 9 Results of 3-bit three-stages DCO for Control Word [000] **a** Output frequency, **b** frequency spectrum with fundamental frequency at 3.52 GHz

delay cell provides an additional tuning approach with a variable capacitor as compared to the standard inverter-based delay cell. Tuning of frequency without varying the power supply voltage provides the advantages of low power consumption. The last stage of the proposed circuits is designed with a 3-T NAND gate which has been implemented with the minimum number of transistors as compared to the standard approach. For a fair comparison for proposed DCO structure with those implemented using inverter-based delay cells only, a comparison based on parameters like output frequency, power consumption has been provided in Table 5.

4 Conclusions

We have proposed a delay cell with NMOS switching network with NMOS varactor acting as a shunt-capacitive loads which exhibits low power consumption and wide output frequency tuning range. The three variants of the proposed DCO were designed in CMOS 0.18 μm

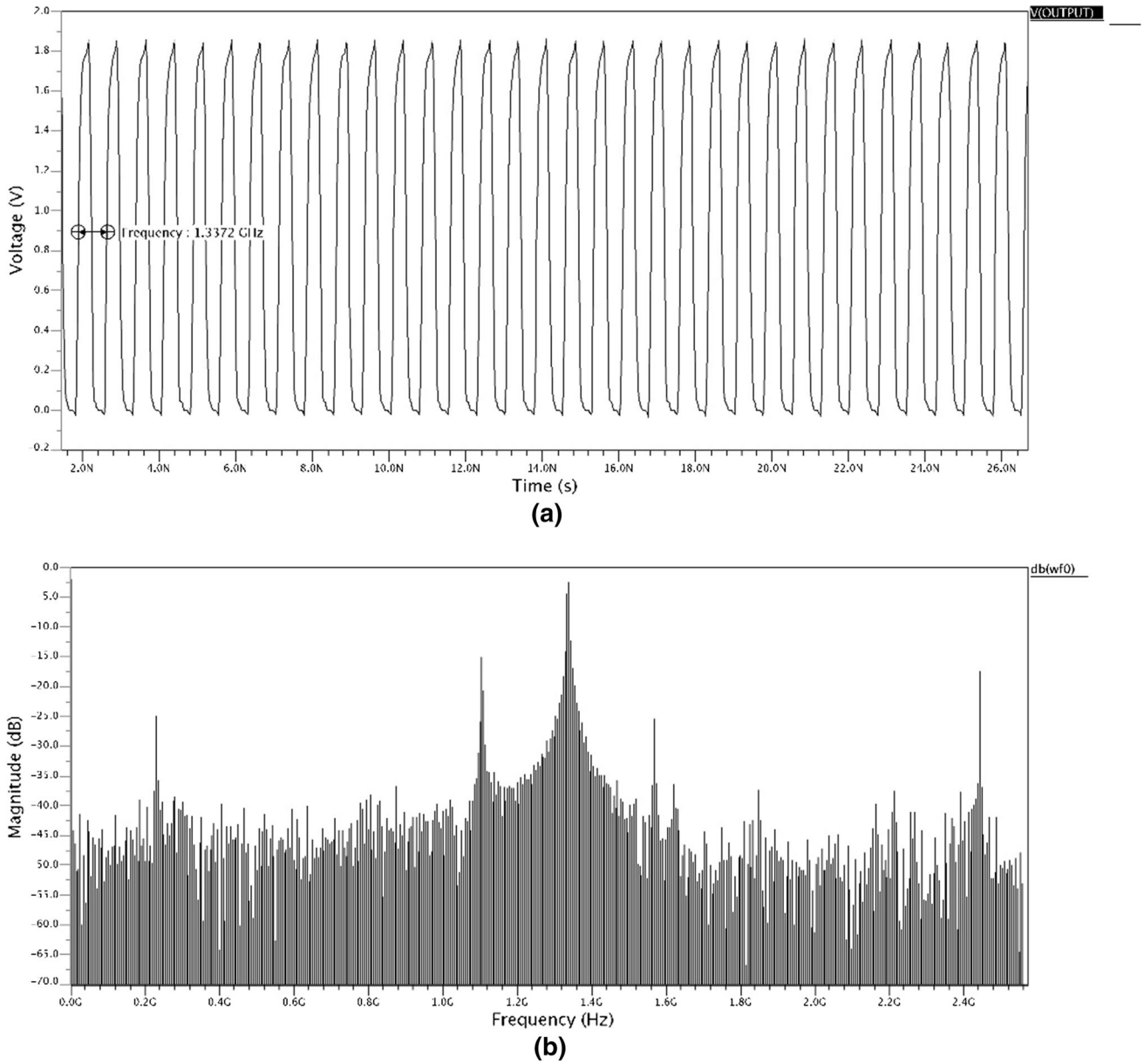

Fig. 10 Results of 3-bit five-stages DCO for Control Word [101] **a** Output frequency, **b** frequency spectrum with fundamental frequency at 1.33 GHz

technology. At 1.8 V supply voltage, 3-bit three-stages DCO circuit reports a wide range of tuning from 1.986 to 3.526 GHz with a power consumption of 1.484 mW. A 3-bit five-stages DCO shows the output frequency from 1.154 to 2.210 GHz and power consumption of 2.762 mW. A 7-stages DCO exhibits an output oscillation frequency variation in the range from 0.835 to 1.658 GHz with a power consumption of 4.04 mW. Phase noise results of the proposed DCOs variants have also been obtained. Three, five and seven-stages DCO show phase noise of − 100.06 dBc/Hz, − 102.08 dBc/Hz and − 105.52 dBc/Hz at 1 MHz respectively. In addition to this, the figure of merit (FoM) for 3,5 and 7-stages was also calculated which comes out to be 165.37 dBc/Hz,160.92 dBc/Hz and 159.07 dBc/Hz respectively. The digital tuning range for 3,5, and 7-stages DCO is 55.96, 62.78, and 66.05% respectively and the DCO has a maximum supply voltage tuning range of 101.45% with the variation of V_{DD} from 1 to 1.8 V. A comparison with earlier published work has been done. The proposed circuit provides a wide tuning range with low power consumption.

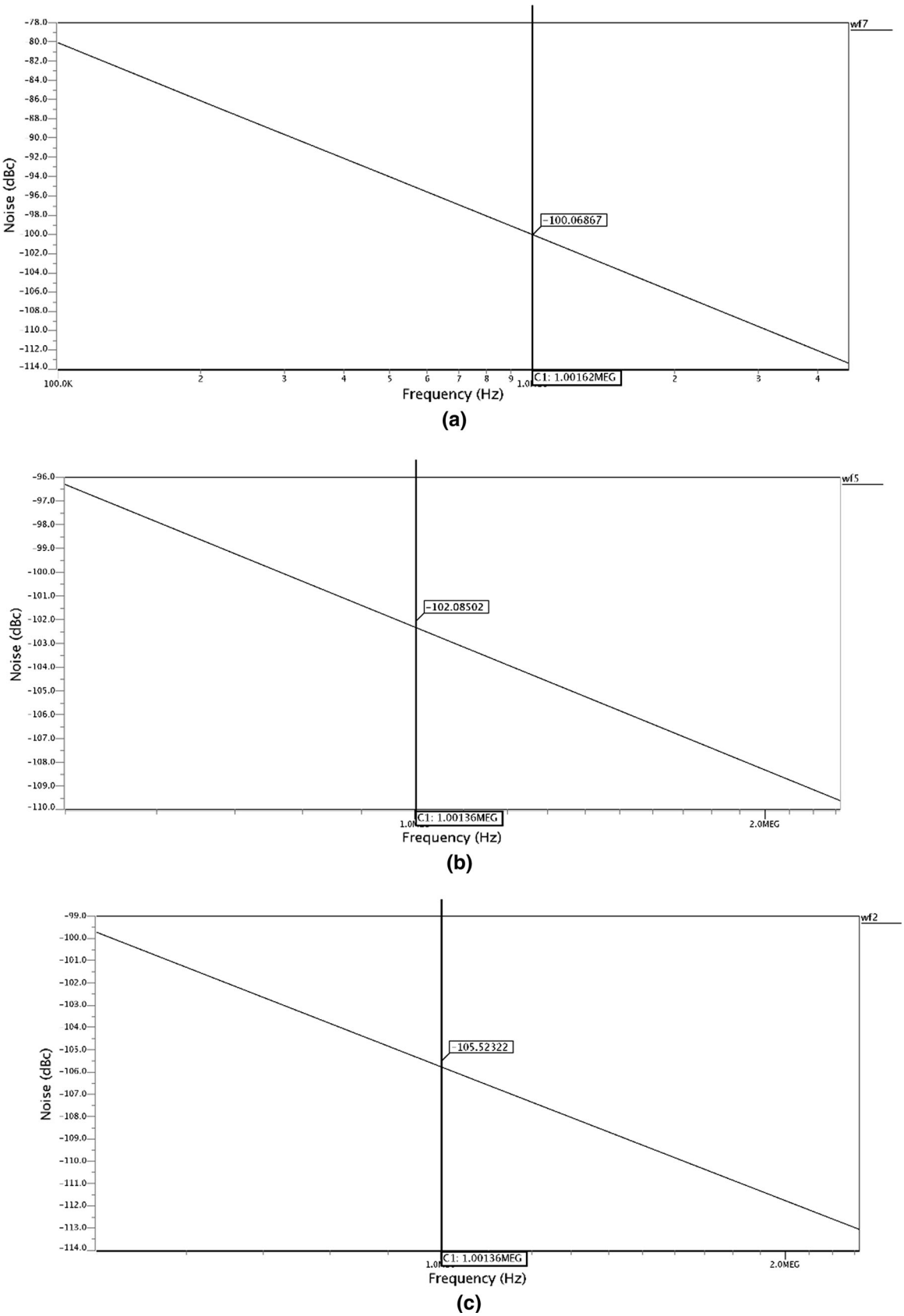

Fig. 11 Phase noise of 3-bit DCO for **a** 3-stages, **b** 5-stages, **c** 7-stages

Table 4 Phase noise and FoM results of the proposed DCO

DCO types	Power supply V_{DD}	Digital tuning range (%)	Phase noise of VCO@1 MHz (dBc/Hz)	FoM (dBc/Hz)	Power consumption (mW)
3-Stages	1.8 V	55.96	− 100.06	165.37	1.484
5-Stages	1.8 V	62.78	− 102.08	160.92	2.762
7-Stages	1.8 V	66.05	− 105.52	159.07	4.040

Table 5 Comparison with earlier published results

DCO Structures	Output frequency (GHz)	CMOS technology (μm)	Phase noise (dBc/Hz)	Power consumption
Reference [7]	0.152–0.366	0.35	–	8.1–24mW
Reference [11]	0.333–1.472	0.35	− 106 @ 1 MHz	63.4 mW
Reference [12]	0.140–1.030	0.18	–	100 mW
Reference [16]	1.350–4.550	0.18	–	–
Reference [18]	2.4	0.13	− 112 @ 500 kHz	–
Proposed 3-bit 3-stages	3.526–1.986	0.18	− 100.0686 dBc/Hz at 1 MHz	1.484 mW
Proposed 3-bit 5-stages	2.210–1.154	0.18	− 102.0850 dBc/Hz at 1 MHz	2.762 mW
Proposed 3-bit 7-stages	1.658–0.835	0.18	− 105.5232 dBc/Hz at 1 MHz	4.040 mW

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